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;Supported Devices:

; EFM8BB31F16G

; EFM8BB31F16G

; EFM8BB31F16G

; EFM8BB31F16G

; EFM8BB31F16I

; EFM8BB31F16I

; EFM8BB31F16I

; EFM8BB31F16I

; EFM8BB31F32G

; EFM8BB31F32G

; EFM8BB31F32G

; EFM8BB31F32G

; EFM8BB31F32I

; EFM8BB31F32I

; EFM8BB31F32I

; EFM8BB31F32I

; EFM8BB31F64G

; EFM8BB31F64G

; EFM8BB31F64G

; EFM8BB31F64G

; EFM8BB31F64I

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; EFM8BB31F64I

; EFM8BB31F64I

;------------------------------------------------------------------------------

; ADC0ASAH Enums (ADC0 Autoscan Start Address High Byte @ 0xB6)

;------------------------------------------------------------------------------

ADC0ASAH\_STADDRH\_\_FMASK EQU 00FH ; Start Address High

ADC0ASAH\_STADDRH\_\_SHIFT EQU 000H ; Start Address High

;------------------------------------------------------------------------------

; ADC0ASAL Enums (ADC0 Autoscan Start Address Low Byte @ 0xB5)

;------------------------------------------------------------------------------

ADC0ASAL\_ENDIAN\_\_BMASK EQU 001H ; Endianness Control

ADC0ASAL\_ENDIAN\_\_SHIFT EQU 000H ; Endianness Control

ADC0ASAL\_ENDIAN\_\_BIG\_ENDIAN EQU 000H ; ADC results in XRAM are stored in big-endian

; order. This will result in the most significant

; byte stored in the even-numbered address.

ADC0ASAL\_ENDIAN\_\_LITTLE\_ENDIAN EQU 001H ; ADC results in XRAM are stored in little-endian

; order. This will result in the most significant

; byte stored in the odd-numbered address.

ADC0ASAL\_STADDRL\_\_FMASK EQU 0FEH ; Start Address Low

ADC0ASAL\_STADDRL\_\_SHIFT EQU 001H ; Start Address Low

;------------------------------------------------------------------------------

; ADC0ASCF Enums (ADC0 Autoscan Configuration @ 0xA1)

;------------------------------------------------------------------------------

ADC0ASCF\_NASCH\_\_FMASK EQU 003H ; Number of Autoscan Channels

ADC0ASCF\_NASCH\_\_SHIFT EQU 000H ; Number of Autoscan Channels

ADC0ASCF\_NASCH\_\_ONE EQU 000H ; Autoscan will only use the ADC0MX setting

; directly.

ADC0ASCF\_NASCH\_\_TWO EQU 001H ; Autoscan will alternate between ADC0MX and

; ADC0MX+1.

ADC0ASCF\_NASCH\_\_THREE EQU 002H ; Autoscan will cycle through ADC0MX, ADC0MX+1 and

; ADC0MX+2.

ADC0ASCF\_NASCH\_\_FOUR EQU 003H ; Autoscan will cycle through ADC0MX, ADC0MX+1,

; ADC0MX+2, and ADC0MX+3.

ADC0ASCF\_ASACT\_\_BMASK EQU 020H ; Autoscan Active

ADC0ASCF\_ASACT\_\_SHIFT EQU 005H ; Autoscan Active

ADC0ASCF\_ASACT\_\_NOT\_ACTIVE EQU 000H ; No scan is in progress.

ADC0ASCF\_ASACT\_\_ACTIVE EQU 020H ; A scan is in progress.

ADC0ASCF\_STEN\_\_BMASK EQU 040H ; Autoscan Single Trigger Enable

ADC0ASCF\_STEN\_\_SHIFT EQU 006H ; Autoscan Single Trigger Enable

ADC0ASCF\_STEN\_\_MULTIPLE\_TRIGGERS EQU 000H ; Each conversion in a scan requires a new

; conversion trigger from the selected conversion

; trigger source.

ADC0ASCF\_STEN\_\_SINGLE\_TRIGGER EQU 040H ; The selected conversion trigger source will begin

; each scan cycle. All conversions within a scan

; cycle are performed automatically when the

; previous conversion is complete.

ADC0ASCF\_ASEN\_\_BMASK EQU 080H ; Autoscan Enable

ADC0ASCF\_ASEN\_\_SHIFT EQU 007H ; Autoscan Enable

ADC0ASCF\_ASEN\_\_HALT\_SCAN EQU 000H ; Clearing to 0 will halt scan operations once any

; pending scan is complete.

ADC0ASCF\_ASEN\_\_START\_SCAN EQU 080H ; Setting to 1 will initialize a scan operation. If

; set to 1 at the end of a scan, a new scan will

; begin.

;------------------------------------------------------------------------------

; ADC0ASCT Enums (ADC0 Autoscan Output Count @ 0xC7)

;------------------------------------------------------------------------------

ADC0ASCT\_ASCNT\_\_FMASK EQU 03FH ; Autoscan Output Count

ADC0ASCT\_ASCNT\_\_SHIFT EQU 000H ; Autoscan Output Count

;------------------------------------------------------------------------------

; ADC0CF0 Enums (ADC0 Configuration @ 0xBC)

;------------------------------------------------------------------------------

ADC0CF0\_ADCLKSEL\_\_BMASK EQU 004H ; ADC Clock Select

ADC0CF0\_ADCLKSEL\_\_SHIFT EQU 002H ; ADC Clock Select

ADC0CF0\_ADCLKSEL\_\_SYSCLK EQU 000H ; ADCCLK = SYSCLK.

ADC0CF0\_ADCLKSEL\_\_HFOSC0 EQU 004H ; ADCCLK = HFOSC0.

ADC0CF0\_ADSC\_\_FMASK EQU 0F8H ; SAR Clock Divider

ADC0CF0\_ADSC\_\_SHIFT EQU 003H ; SAR Clock Divider

;------------------------------------------------------------------------------

; ADC0CF1 Enums (ADC0 Configuration @ 0xB9)

;------------------------------------------------------------------------------

ADC0CF1\_ADTK\_\_FMASK EQU 03FH ; Conversion Tracking Time

ADC0CF1\_ADTK\_\_SHIFT EQU 000H ; Conversion Tracking Time

ADC0CF1\_ADLPM\_\_BMASK EQU 080H ; Low Power Mode Enable

ADC0CF1\_ADLPM\_\_SHIFT EQU 007H ; Low Power Mode Enable

ADC0CF1\_ADLPM\_\_LP\_DISABLED EQU 000H ; Disable low power mode.

ADC0CF1\_ADLPM\_\_LP\_ENABLED EQU 080H ; Enable low power mode.

;------------------------------------------------------------------------------

; ADC0CF2 Enums (ADC0 Power Control @ 0xDF)

;------------------------------------------------------------------------------

ADC0CF2\_ADPWR\_\_FMASK EQU 01FH ; Power Up Delay Time

ADC0CF2\_ADPWR\_\_SHIFT EQU 000H ; Power Up Delay Time

ADC0CF2\_REFSL\_\_FMASK EQU 060H ; Voltage Reference Select

ADC0CF2\_REFSL\_\_SHIFT EQU 005H ; Voltage Reference Select

ADC0CF2\_REFSL\_\_VREF\_PIN EQU 000H ; The ADC0 voltage reference is the VREF pin

; (external or from the on-chip reference).

ADC0CF2\_REFSL\_\_VDD\_PIN EQU 020H ; The ADC0 voltage reference is the VDD pin.

ADC0CF2\_REFSL\_\_INTERNAL\_LDO EQU 040H ; The ADC0 voltage reference is the internal 1.8 V

; digital supply voltage.

ADC0CF2\_REFSL\_\_INTERNAL\_VREF EQU 060H ; The ADC0 voltage reference is the internal voltage

; reference.

ADC0CF2\_GNDSL\_\_BMASK EQU 080H ; Analog Ground Reference

ADC0CF2\_GNDSL\_\_SHIFT EQU 007H ; Analog Ground Reference

ADC0CF2\_GNDSL\_\_GND\_PIN EQU 000H ; The ADC0 ground reference is the GND pin.

ADC0CF2\_GNDSL\_\_AGND\_PIN EQU 080H ; The ADC0 ground reference is the AGND pin.

;------------------------------------------------------------------------------

; ADC0CN0 Enums (ADC0 Control 0 @ 0xE8)

;------------------------------------------------------------------------------

ADC0CN0\_TEMPE\_\_BMASK EQU 001H ; Temperature Sensor Enable

ADC0CN0\_TEMPE\_\_SHIFT EQU 000H ; Temperature Sensor Enable

ADC0CN0\_TEMPE\_\_TEMP\_DISABLED EQU 000H ; Disable the Temperature Sensor.

ADC0CN0\_TEMPE\_\_TEMP\_ENABLED EQU 001H ; Enable the Temperature Sensor.

ADC0CN0\_ADGN\_\_FMASK EQU 006H ; Gain Control

ADC0CN0\_ADGN\_\_SHIFT EQU 001H ; Gain Control

ADC0CN0\_ADGN\_\_GAIN\_1 EQU 000H ; The on-chip PGA gain is 1.

ADC0CN0\_ADGN\_\_GAIN\_0P75 EQU 002H ; The on-chip PGA gain is 0.75.

ADC0CN0\_ADGN\_\_GAIN\_0P5 EQU 004H ; The on-chip PGA gain is 0.5.

ADC0CN0\_ADGN\_\_GAIN\_0P25 EQU 006H ; The on-chip PGA gain is 0.25.

ADC0CN0\_ADWINT\_\_BMASK EQU 008H ; Window Compare Interrupt Flag

ADC0CN0\_ADWINT\_\_SHIFT EQU 003H ; Window Compare Interrupt Flag

ADC0CN0\_ADWINT\_\_NOT\_SET EQU 000H ; An ADC window compare event did not occur.

ADC0CN0\_ADWINT\_\_SET EQU 008H ; An ADC window compare event occurred.

ADC0CN0\_ADBUSY\_\_BMASK EQU 010H ; ADC Busy

ADC0CN0\_ADBUSY\_\_SHIFT EQU 004H ; ADC Busy

ADC0CN0\_ADBUSY\_\_NOT\_SET EQU 000H ; An ADC0 conversion is not currently in progress.

ADC0CN0\_ADBUSY\_\_SET EQU 010H ; ADC0 conversion is in progress or start an ADC0

; conversion.

ADC0CN0\_ADINT\_\_BMASK EQU 020H ; Conversion Complete Interrupt Flag

ADC0CN0\_ADINT\_\_SHIFT EQU 005H ; Conversion Complete Interrupt Flag

ADC0CN0\_ADINT\_\_NOT\_SET EQU 000H ; ADC0 has not completed a conversion since the last

; time ADINT was cleared.

ADC0CN0\_ADINT\_\_SET EQU 020H ; ADC0 completed a data conversion.

ADC0CN0\_IPOEN\_\_BMASK EQU 040H ; Idle Powered-off Enable

ADC0CN0\_IPOEN\_\_SHIFT EQU 006H ; Idle Powered-off Enable

ADC0CN0\_IPOEN\_\_ALWAYS\_ON EQU 000H ; Keep ADC powered on when ADEN is 1.

ADC0CN0\_IPOEN\_\_POWER\_DOWN EQU 040H ; Power down when ADC is idle (not converting).

ADC0CN0\_ADEN\_\_BMASK EQU 080H ; ADC Enable

ADC0CN0\_ADEN\_\_SHIFT EQU 007H ; ADC Enable

ADC0CN0\_ADEN\_\_DISABLED EQU 000H ; Disable ADC0 (low-power shutdown).

ADC0CN0\_ADEN\_\_ENABLED EQU 080H ; Enable ADC0 (active and ready for data

; conversions).

;------------------------------------------------------------------------------

; ADC0CN1 Enums (ADC0 Control 1 @ 0xB2)

;------------------------------------------------------------------------------

ADC0CN1\_ADRPT\_\_FMASK EQU 007H ; Repeat Count

ADC0CN1\_ADRPT\_\_SHIFT EQU 000H ; Repeat Count

ADC0CN1\_ADRPT\_\_ACC\_1 EQU 000H ; Perform and Accumulate 1 conversion.

ADC0CN1\_ADRPT\_\_ACC\_4 EQU 001H ; Perform and Accumulate 4 conversions.

ADC0CN1\_ADRPT\_\_ACC\_8 EQU 002H ; Perform and Accumulate 8 conversions.

ADC0CN1\_ADRPT\_\_ACC\_16 EQU 003H ; Perform and Accumulate 16 conversions.

ADC0CN1\_ADRPT\_\_ACC\_32 EQU 004H ; Perform and Accumulate 32 conversions.

ADC0CN1\_ADSJST\_\_FMASK EQU 038H ; Accumulator Shift and Justify

ADC0CN1\_ADSJST\_\_SHIFT EQU 003H ; Accumulator Shift and Justify

ADC0CN1\_ADSJST\_\_RIGHT\_NO\_SHIFT EQU 000H ; Right justified. No shifting applied.

ADC0CN1\_ADSJST\_\_RIGHT\_SHIFT\_1 EQU 008H ; Right justified. Shifted right by 1 bit.

ADC0CN1\_ADSJST\_\_RIGHT\_SHIFT\_2 EQU 010H ; Right justified. Shifted right by 2 bits.

ADC0CN1\_ADSJST\_\_RIGHT\_SHIFT\_3 EQU 018H ; Right justified. Shifted right by 3 bits.

ADC0CN1\_ADBITS\_\_FMASK EQU 0C0H ; Resolution Control

ADC0CN1\_ADBITS\_\_SHIFT EQU 006H ; Resolution Control

ADC0CN1\_ADBITS\_\_10\_BIT EQU 000H ; ADC0 operates in 10-bit mode.

ADC0CN1\_ADBITS\_\_12\_BIT EQU 040H ; ADC0 operates in 12-bit mode.

;------------------------------------------------------------------------------

; ADC0CN2 Enums (ADC0 Control 2 @ 0xB3)

;------------------------------------------------------------------------------

ADC0CN2\_ADCM\_\_FMASK EQU 00FH ; Start of Conversion Mode Select

ADC0CN2\_ADCM\_\_SHIFT EQU 000H ; Start of Conversion Mode Select

ADC0CN2\_ADCM\_\_ADBUSY EQU 000H ; ADC0 conversion initiated on write of 1 to ADBUSY.

ADC0CN2\_ADCM\_\_TIMER0 EQU 001H ; ADC0 conversion initiated on overflow of Timer 0.

ADC0CN2\_ADCM\_\_TIMER2 EQU 002H ; ADC0 conversion initiated on overflow of Timer 2.

ADC0CN2\_ADCM\_\_TIMER3 EQU 003H ; ADC0 conversion initiated on overflow of Timer 3.

ADC0CN2\_ADCM\_\_CNVSTR EQU 004H ; ADC0 conversion initiated on rising edge of

; CNVSTR.

ADC0CN2\_ADCM\_\_CEX5 EQU 005H ; ADC0 conversion initiated on rising edge of CEX5.

ADC0CN2\_ADCM\_\_TIMER4 EQU 006H ; ADC0 conversion initiated on overflow of Timer 4.

ADC0CN2\_ADCM\_\_TIMER5 EQU 007H ; ADC0 conversion initiated on overflow of Timer 5.

ADC0CN2\_ADCM\_\_CLU0 EQU 008H ; ADC0 conversion initiated on CLU0 Output.

ADC0CN2\_ADCM\_\_CLU1 EQU 009H ; ADC0 conversion initiated on CLU1 Output.

ADC0CN2\_ADCM\_\_CLU2 EQU 00AH ; ADC0 conversion initiated on CLU2 Output.

ADC0CN2\_ADCM\_\_CLU3 EQU 00BH ; ADC0 conversion initiated on CLU3 Output.

ADC0CN2\_PACEN\_\_BMASK EQU 080H ; Preserve Accumulator Enable

ADC0CN2\_PACEN\_\_SHIFT EQU 007H ; Preserve Accumulator Enable

ADC0CN2\_PACEN\_\_PAC\_DISABLED EQU 000H ; The ADC accumulator is over-written with the

; results of any conversion (or set of conversions

; as specified by ADRPT).

ADC0CN2\_PACEN\_\_PAC\_ENABLED EQU 080H ; The ADC accumulator always adds new results to the

; existing output. The accumulator is never cleared

; in this mode.

;------------------------------------------------------------------------------

; ADC0GTH Enums (ADC0 Greater-Than High Byte @ 0xC4)

;------------------------------------------------------------------------------

ADC0GTH\_ADC0GTH\_\_FMASK EQU 0FFH ; Greater-Than High Byte

ADC0GTH\_ADC0GTH\_\_SHIFT EQU 000H ; Greater-Than High Byte

;------------------------------------------------------------------------------

; ADC0GTL Enums (ADC0 Greater-Than Low Byte @ 0xC3)

;------------------------------------------------------------------------------

ADC0GTL\_ADC0GTL\_\_FMASK EQU 0FFH ; Greater-Than Low Byte

ADC0GTL\_ADC0GTL\_\_SHIFT EQU 000H ; Greater-Than Low Byte

;------------------------------------------------------------------------------

; ADC0H Enums (ADC0 Data Word High Byte @ 0xBE)

;------------------------------------------------------------------------------

ADC0H\_ADC0H\_\_FMASK EQU 0FFH ; Data Word High Byte

ADC0H\_ADC0H\_\_SHIFT EQU 000H ; Data Word High Byte

;------------------------------------------------------------------------------

; ADC0L Enums (ADC0 Data Word Low Byte @ 0xBD)

;------------------------------------------------------------------------------

ADC0L\_ADC0L\_\_FMASK EQU 0FFH ; Data Word Low Byte

ADC0L\_ADC0L\_\_SHIFT EQU 000H ; Data Word Low Byte

;------------------------------------------------------------------------------

; ADC0LTH Enums (ADC0 Less-Than High Byte @ 0xC6)

;------------------------------------------------------------------------------

ADC0LTH\_ADC0LTH\_\_FMASK EQU 0FFH ; Less-Than High Byte

ADC0LTH\_ADC0LTH\_\_SHIFT EQU 000H ; Less-Than High Byte

;------------------------------------------------------------------------------

; ADC0LTL Enums (ADC0 Less-Than Low Byte @ 0xC5)

;------------------------------------------------------------------------------

ADC0LTL\_ADC0LTL\_\_FMASK EQU 0FFH ; Less-Than Low Byte

ADC0LTL\_ADC0LTL\_\_SHIFT EQU 000H ; Less-Than Low Byte

;------------------------------------------------------------------------------

; ADC0MX Enums (ADC0 Multiplexer Selection @ 0xBB)

;------------------------------------------------------------------------------

ADC0MX\_ADC0MX\_\_FMASK EQU 01FH ; AMUX0 Positive Input Selection

ADC0MX\_ADC0MX\_\_SHIFT EQU 000H ; AMUX0 Positive Input Selection

ADC0MX\_ADC0MX\_\_ADC0P0 EQU 000H ; Select ADC0.0.

ADC0MX\_ADC0MX\_\_ADC0P1 EQU 001H ; Select ADC0.1.

ADC0MX\_ADC0MX\_\_ADC0P2 EQU 002H ; Select ADC0.2.

ADC0MX\_ADC0MX\_\_ADC0P3 EQU 003H ; Select ADC0.3.

ADC0MX\_ADC0MX\_\_ADC0P4 EQU 004H ; Select ADC0.4.

ADC0MX\_ADC0MX\_\_ADC0P5 EQU 005H ; Select ADC0.5.

ADC0MX\_ADC0MX\_\_ADC0P6 EQU 006H ; Select ADC0.6.

ADC0MX\_ADC0MX\_\_ADC0P7 EQU 007H ; Select ADC0.7.

ADC0MX\_ADC0MX\_\_ADC0P8 EQU 008H ; Select ADC0.8.

ADC0MX\_ADC0MX\_\_ADC0P9 EQU 009H ; Select ADC0.9.

ADC0MX\_ADC0MX\_\_ADC0P10 EQU 00AH ; Select ADC0.10.

ADC0MX\_ADC0MX\_\_ADC0P11 EQU 00BH ; Select ADC0.11.

ADC0MX\_ADC0MX\_\_ADC0P12 EQU 00CH ; Select ADC0.12.

ADC0MX\_ADC0MX\_\_ADC0P13 EQU 00DH ; Select ADC0.13.

ADC0MX\_ADC0MX\_\_ADC0P14 EQU 00EH ; Select ADC0.14.

ADC0MX\_ADC0MX\_\_ADC0P15 EQU 00FH ; Select ADC0.15.

ADC0MX\_ADC0MX\_\_ADC0P16 EQU 010H ; Select ADC0.16.

ADC0MX\_ADC0MX\_\_ADC0P17 EQU 011H ; Select ADC0.17.

ADC0MX\_ADC0MX\_\_ADC0P18 EQU 012H ; Select ADC0.18.

ADC0MX\_ADC0MX\_\_ADC0P19 EQU 013H ; Select ADC0.19.

ADC0MX\_ADC0MX\_\_TEMP EQU 014H ; Select ADC0.20

ADC0MX\_ADC0MX\_\_LDO\_OUT EQU 015H ; Select ADC0.21

ADC0MX\_ADC0MX\_\_VDD EQU 016H ; Select ADC0.22

ADC0MX\_ADC0MX\_\_GND EQU 017H ; Select ADC0.23

ADC0MX\_ADC0MX\_\_NONE EQU 01FH ; No input selected.

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; ACC Enums (Accumulator @ 0xE0)

;------------------------------------------------------------------------------

ACC\_ACC\_\_FMASK EQU 0FFH ; Accumulator

ACC\_ACC\_\_SHIFT EQU 000H ; Accumulator

;------------------------------------------------------------------------------

; B Enums (B Register @ 0xF0)

;------------------------------------------------------------------------------

B\_B\_\_FMASK EQU 0FFH ; B Register

B\_B\_\_SHIFT EQU 000H ; B Register

;------------------------------------------------------------------------------

; DPH Enums (Data Pointer High @ 0x83)

;------------------------------------------------------------------------------

DPH\_DPH\_\_FMASK EQU 0FFH ; Data Pointer High

DPH\_DPH\_\_SHIFT EQU 000H ; Data Pointer High

;------------------------------------------------------------------------------

; DPL Enums (Data Pointer Low @ 0x82)

;------------------------------------------------------------------------------

DPL\_DPL\_\_FMASK EQU 0FFH ; Data Pointer Low

DPL\_DPL\_\_SHIFT EQU 000H ; Data Pointer Low

;------------------------------------------------------------------------------

; PFE0CN Enums (Prefetch Engine Control @ 0xC1)

;------------------------------------------------------------------------------

PFE0CN\_FLRT\_\_FMASK EQU 030H ; Flash Read Timing

PFE0CN\_FLRT\_\_SHIFT EQU 004H ; Flash Read Timing

PFE0CN\_FLRT\_\_SYSCLK\_BELOW\_25\_MHZ EQU 000H ; SYSCLK < 25 MHz.

PFE0CN\_FLRT\_\_SYSCLK\_BELOW\_50\_MHZ EQU 010H ; SYSCLK < 50 MHz.

;------------------------------------------------------------------------------

; PSW Enums (Program Status Word @ 0xD0)

;------------------------------------------------------------------------------

PSW\_PARITY\_\_BMASK EQU 001H ; Parity Flag

PSW\_PARITY\_\_SHIFT EQU 000H ; Parity Flag

PSW\_PARITY\_\_NOT\_SET EQU 000H ; The sum of the 8 bits in the accumulator is even.

PSW\_PARITY\_\_SET EQU 001H ; The sum of the 8 bits in the accumulator is odd.

PSW\_F1\_\_BMASK EQU 002H ; User Flag 1

PSW\_F1\_\_SHIFT EQU 001H ; User Flag 1

PSW\_F1\_\_NOT\_SET EQU 000H ; Flag is not set.

PSW\_F1\_\_SET EQU 002H ; Flag is set.

PSW\_OV\_\_BMASK EQU 004H ; Overflow Flag

PSW\_OV\_\_SHIFT EQU 002H ; Overflow Flag

PSW\_OV\_\_NOT\_SET EQU 000H ; An overflow did not occur.

PSW\_OV\_\_SET EQU 004H ; An overflow occurred.

PSW\_RS\_\_FMASK EQU 018H ; Register Bank Select

PSW\_RS\_\_SHIFT EQU 003H ; Register Bank Select

PSW\_RS\_\_BANK0 EQU 000H ; Bank 0, Addresses 0x00-0x07

PSW\_RS\_\_BANK1 EQU 008H ; Bank 1, Addresses 0x08-0x0F

PSW\_RS\_\_BANK2 EQU 010H ; Bank 2, Addresses 0x10-0x17

PSW\_RS\_\_BANK3 EQU 018H ; Bank 3, Addresses 0x18-0x1F

PSW\_F0\_\_BMASK EQU 020H ; User Flag 0

PSW\_F0\_\_SHIFT EQU 005H ; User Flag 0

PSW\_F0\_\_NOT\_SET EQU 000H ; Flag is not set.

PSW\_F0\_\_SET EQU 020H ; Flag is set.

PSW\_AC\_\_BMASK EQU 040H ; Auxiliary Carry Flag

PSW\_AC\_\_SHIFT EQU 006H ; Auxiliary Carry Flag

PSW\_AC\_\_NOT\_SET EQU 000H ; A carry into (addition) or borrow from

; (subtraction) the high order nibble did not occur.

PSW\_AC\_\_SET EQU 040H ; A carry into (addition) or borrow from

; (subtraction) the high order nibble occurred.

PSW\_CY\_\_BMASK EQU 080H ; Carry Flag

PSW\_CY\_\_SHIFT EQU 007H ; Carry Flag

PSW\_CY\_\_NOT\_SET EQU 000H ; A carry (addition) or borrow (subtraction) did not

; occur.

PSW\_CY\_\_SET EQU 080H ; A carry (addition) or borrow (subtraction)

; occurred.

;------------------------------------------------------------------------------

; SP Enums (Stack Pointer @ 0x81)

;------------------------------------------------------------------------------

SP\_SP\_\_FMASK EQU 0FFH ; Stack Pointer

SP\_SP\_\_SHIFT EQU 000H ; Stack Pointer

;------------------------------------------------------------------------------

; CLKSEL Enums (Clock Select @ 0xA9)

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CLKSEL\_CLKSL\_\_FMASK EQU 007H ; Clock Source Select

CLKSEL\_CLKSL\_\_SHIFT EQU 000H ; Clock Source Select

CLKSEL\_CLKSL\_\_HFOSC0 EQU 000H ; Clock derived from the Internal High Frequency

; Oscillator 0.

CLKSEL\_CLKSL\_\_EXTOSC EQU 001H ; Clock derived from the External Oscillator

; circuit.

CLKSEL\_CLKSL\_\_LFOSC EQU 002H ; Clock derived from the Internal Low-Frequency

; Oscillator.

CLKSEL\_CLKSL\_\_HFOSC1 EQU 003H ; Clock derived from the Internal High Frequency

; Oscillator 1.

CLKSEL\_CLKSL\_\_HFOSC0\_DIV\_1P5 EQU 004H ; Clock derived from the Internal High Frequency

; Oscillator 0, pre-scaled by 1.5.

CLKSEL\_CLKSL\_\_HFOSC1\_DIV\_1P5 EQU 007H ; Clock derived from the Internal High Frequency

; Oscillator 1, pre-scaled by 1.5.

CLKSEL\_CLKDIV\_\_FMASK EQU 070H ; Clock Source Divider

CLKSEL\_CLKDIV\_\_SHIFT EQU 004H ; Clock Source Divider

CLKSEL\_CLKDIV\_\_SYSCLK\_DIV\_1 EQU 000H ; SYSCLK is equal to selected clock source divided

; by 1.

CLKSEL\_CLKDIV\_\_SYSCLK\_DIV\_2 EQU 010H ; SYSCLK is equal to selected clock source divided

; by 2.

CLKSEL\_CLKDIV\_\_SYSCLK\_DIV\_4 EQU 020H ; SYSCLK is equal to selected clock source divided

; by 4.

CLKSEL\_CLKDIV\_\_SYSCLK\_DIV\_8 EQU 030H ; SYSCLK is equal to selected clock source divided

; by 8.

CLKSEL\_CLKDIV\_\_SYSCLK\_DIV\_16 EQU 040H ; SYSCLK is equal to selected clock source divided

; by 16.

CLKSEL\_CLKDIV\_\_SYSCLK\_DIV\_32 EQU 050H ; SYSCLK is equal to selected clock source divided

; by 32.

CLKSEL\_CLKDIV\_\_SYSCLK\_DIV\_64 EQU 060H ; SYSCLK is equal to selected clock source divided

; by 64.

CLKSEL\_CLKDIV\_\_SYSCLK\_DIV\_128 EQU 070H ; SYSCLK is equal to selected clock source divided

; by 128.

CLKSEL\_DIVRDY\_\_BMASK EQU 080H ; Clock Divider Ready

CLKSEL\_DIVRDY\_\_SHIFT EQU 007H ; Clock Divider Ready

CLKSEL\_DIVRDY\_\_NOT\_READY EQU 000H ; Clock has not propagated through divider yet.

CLKSEL\_DIVRDY\_\_READY EQU 080H ; Clock has propagated through divider.

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; CLU0CF Enums (Configurable Logic Unit 0 Configuration @ 0xB1)

;------------------------------------------------------------------------------

CLU0CF\_CLKSEL\_\_FMASK EQU 003H ; CLU D flip-flop Clock Selection

CLU0CF\_CLKSEL\_\_SHIFT EQU 000H ; CLU D flip-flop Clock Selection

CLU0CF\_CLKSEL\_\_CARRY\_IN EQU 000H ; The carry-in signal.

CLU0CF\_CLKSEL\_\_MXA\_INPUT EQU 001H ; The MXA input.

CLU0CF\_CLKSEL\_\_SYSCLK EQU 002H ; SYSCLK.

CLU0CF\_CLKSEL\_\_ALTCLK EQU 003H ; The alternate clock signal CLU0ALTCLK.

CLU0CF\_CLKINV\_\_BMASK EQU 004H ; CLU D flip-flop Clock Invert

CLU0CF\_CLKINV\_\_SHIFT EQU 002H ; CLU D flip-flop Clock Invert

CLU0CF\_CLKINV\_\_NORMAL EQU 000H ; Clock signal is not inverted.

CLU0CF\_CLKINV\_\_INVERT EQU 004H ; Clock signal will be inverted.

CLU0CF\_RST\_\_BMASK EQU 008H ; CLU D flip-flop Reset

CLU0CF\_RST\_\_SHIFT EQU 003H ; CLU D flip-flop Reset

CLU0CF\_RST\_\_RESET EQU 008H ; Reset the flip flop.

CLU0CF\_OEN\_\_BMASK EQU 040H ; CLU Port Output Enable

CLU0CF\_OEN\_\_SHIFT EQU 006H ; CLU Port Output Enable

CLU0CF\_OEN\_\_DISABLE EQU 000H ; Disables asynchronous output to the selected GPIO

; pin

CLU0CF\_OEN\_\_ENABLE EQU 040H ; Enables asynchronous output to the selected GPIO

; pin

CLU0CF\_OUTSEL\_\_BMASK EQU 080H ; CLU Output Select

CLU0CF\_OUTSEL\_\_SHIFT EQU 007H ; CLU Output Select

CLU0CF\_OUTSEL\_\_D\_FF EQU 000H ; Select D flip-flop output of CLU

CLU0CF\_OUTSEL\_\_LUT EQU 080H ; Select LUT output.

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; CLU0FN Enums (Configurable Logic Unit 0 Function Select @ 0xAF)

;------------------------------------------------------------------------------

CLU0FN\_FNSEL\_\_FMASK EQU 0FFH ; CLU Look-Up-Table function select

CLU0FN\_FNSEL\_\_SHIFT EQU 000H ; CLU Look-Up-Table function select

;------------------------------------------------------------------------------

; CLU0MX Enums (Configurable Logic Unit 0 Multiplexer @ 0x84)

;------------------------------------------------------------------------------

CLU0MX\_MXB\_\_FMASK EQU 00FH ; CLU0 B Input Multiplexer Selection

CLU0MX\_MXB\_\_SHIFT EQU 000H ; CLU0 B Input Multiplexer Selection

CLU0MX\_MXB\_\_CLU0B0 EQU 000H ; Select CLU0B.0

CLU0MX\_MXB\_\_CLU0B1 EQU 001H ; Select CLU0B.1

CLU0MX\_MXB\_\_CLU0B2 EQU 002H ; Select CLU0B.2

CLU0MX\_MXB\_\_CLU0B3 EQU 003H ; Select CLU0B.3

CLU0MX\_MXB\_\_CLU0B4 EQU 004H ; Select CLU0B.4

CLU0MX\_MXB\_\_CLU0B5 EQU 005H ; Select CLU0B.5

CLU0MX\_MXB\_\_CLU0B6 EQU 006H ; Select CLU0B.6

CLU0MX\_MXB\_\_CLU0B7 EQU 007H ; Select CLU0B.7

CLU0MX\_MXB\_\_CLU0B8 EQU 008H ; Select CLU0B.8

CLU0MX\_MXB\_\_CLU0B9 EQU 009H ; Select CLU0B.9

CLU0MX\_MXB\_\_CLU0B10 EQU 00AH ; Select CLU0B.10

CLU0MX\_MXB\_\_CLU0B11 EQU 00BH ; Select CLU0B.11

CLU0MX\_MXB\_\_CLU0B12 EQU 00CH ; Select CLU0B.12

CLU0MX\_MXB\_\_CLU0B13 EQU 00DH ; Select CLU0B.13

CLU0MX\_MXB\_\_CLU0B14 EQU 00EH ; Select CLU0B.14

CLU0MX\_MXB\_\_CLU0B15 EQU 00FH ; Select CLU0B.15

CLU0MX\_MXA\_\_FMASK EQU 0F0H ; CLU0 A Input Multiplexer Selection

CLU0MX\_MXA\_\_SHIFT EQU 004H ; CLU0 A Input Multiplexer Selection

CLU0MX\_MXA\_\_CLU0A0 EQU 000H ; Select CLU0A.0

CLU0MX\_MXA\_\_CLU0A1 EQU 010H ; Select CLU0A.1

CLU0MX\_MXA\_\_CLU0A2 EQU 020H ; Select CLU0A.2

CLU0MX\_MXA\_\_CLU0A3 EQU 030H ; Select CLU0A.3

CLU0MX\_MXA\_\_CLU0A4 EQU 040H ; Select CLU0A.4

CLU0MX\_MXA\_\_CLU0A5 EQU 050H ; Select CLU0A.5

CLU0MX\_MXA\_\_CLU0A6 EQU 060H ; Select CLU0A.6

CLU0MX\_MXA\_\_CLU0A7 EQU 070H ; Select CLU0A.7

CLU0MX\_MXA\_\_CLU0A8 EQU 080H ; Select CLU0A.8

CLU0MX\_MXA\_\_CLU0A9 EQU 090H ; Select CLU0A.9

CLU0MX\_MXA\_\_CLU0A10 EQU 0A0H ; Select CLU0A.10

CLU0MX\_MXA\_\_CLU0A11 EQU 0B0H ; Select CLU0A.11

CLU0MX\_MXA\_\_CLU0A12 EQU 0C0H ; Select CLU0A.12

CLU0MX\_MXA\_\_CLU0A13 EQU 0D0H ; Select CLU0A.13

CLU0MX\_MXA\_\_CLU0A14 EQU 0E0H ; Select CLU0A.14

CLU0MX\_MXA\_\_CLU0A15 EQU 0F0H ; Select CLU0A.15

;------------------------------------------------------------------------------

; CLU1CF Enums (Configurable Logic Unit 1 Configuration @ 0xB3)

;------------------------------------------------------------------------------

CLU1CF\_CLKSEL\_\_FMASK EQU 003H ; CLU D flip-flop Clock Selection

CLU1CF\_CLKSEL\_\_SHIFT EQU 000H ; CLU D flip-flop Clock Selection

CLU1CF\_CLKSEL\_\_CARRY\_IN EQU 000H ; The carry-in signal.

CLU1CF\_CLKSEL\_\_MXA\_INPUT EQU 001H ; The MXA input.

CLU1CF\_CLKSEL\_\_SYSCLK EQU 002H ; SYSCLK.

CLU1CF\_CLKSEL\_\_ALTCLK EQU 003H ; The alternate clock signal CLU1ALTCLK.

CLU1CF\_CLKINV\_\_BMASK EQU 004H ; CLU D flip-flop Clock Invert

CLU1CF\_CLKINV\_\_SHIFT EQU 002H ; CLU D flip-flop Clock Invert

CLU1CF\_CLKINV\_\_NORMAL EQU 000H ; Clock signal is not inverted.

CLU1CF\_CLKINV\_\_INVERT EQU 004H ; Clock signal will be inverted.

CLU1CF\_RST\_\_BMASK EQU 008H ; CLU D flip-flop Reset

CLU1CF\_RST\_\_SHIFT EQU 003H ; CLU D flip-flop Reset

CLU1CF\_RST\_\_RESET EQU 008H ; Reset the flip flop.

CLU1CF\_OEN\_\_BMASK EQU 040H ; CLU Port Output Enable

CLU1CF\_OEN\_\_SHIFT EQU 006H ; CLU Port Output Enable

CLU1CF\_OEN\_\_DISABLE EQU 000H ; Disables asynchronous output to the selected GPIO

; pin

CLU1CF\_OEN\_\_ENABLE EQU 040H ; Enables asynchronous output to the selected GPIO

; pin

CLU1CF\_OUTSEL\_\_BMASK EQU 080H ; CLU Output Select

CLU1CF\_OUTSEL\_\_SHIFT EQU 007H ; CLU Output Select

CLU1CF\_OUTSEL\_\_D\_FF EQU 000H ; Select D flip-flop output of CLU

CLU1CF\_OUTSEL\_\_LUT EQU 080H ; Select LUT output.

;------------------------------------------------------------------------------

; CLU1FN Enums (Configurable Logic Unit 1 Function Select @ 0xB2)

;------------------------------------------------------------------------------

CLU1FN\_FNSEL\_\_FMASK EQU 0FFH ; CLU Look-Up-Table function select

CLU1FN\_FNSEL\_\_SHIFT EQU 000H ; CLU Look-Up-Table function select

;------------------------------------------------------------------------------

; CLU1MX Enums (Configurable Logic Unit 1 Multiplexer @ 0x85)

;------------------------------------------------------------------------------

CLU1MX\_MXB\_\_FMASK EQU 00FH ; CLU1 B Input Multiplexer Selection

CLU1MX\_MXB\_\_SHIFT EQU 000H ; CLU1 B Input Multiplexer Selection

CLU1MX\_MXB\_\_CLU1B0 EQU 000H ; Select CLU1B.0

CLU1MX\_MXB\_\_CLU1B1 EQU 001H ; Select CLU1B.1

CLU1MX\_MXB\_\_CLU1B2 EQU 002H ; Select CLU1B.2

CLU1MX\_MXB\_\_CLU1B3 EQU 003H ; Select CLU1B.3

CLU1MX\_MXB\_\_CLU1B4 EQU 004H ; Select CLU1B.4

CLU1MX\_MXB\_\_CLU1B5 EQU 005H ; Select CLU1B.5

CLU1MX\_MXB\_\_CLU1B6 EQU 006H ; Select CLU1B.6

CLU1MX\_MXB\_\_CLU1B7 EQU 007H ; Select CLU1B.7

CLU1MX\_MXB\_\_CLU1B8 EQU 008H ; Select CLU1B.8

CLU1MX\_MXB\_\_CLU1B9 EQU 009H ; Select CLU1B.9

CLU1MX\_MXB\_\_CLU1B10 EQU 00AH ; Select CLU1B.10

CLU1MX\_MXB\_\_CLU1B11 EQU 00BH ; Select CLU1B.11

CLU1MX\_MXB\_\_CLU1B12 EQU 00CH ; Select CLU1B.12

CLU1MX\_MXB\_\_CLU1B13 EQU 00DH ; Select CLU1B.13

CLU1MX\_MXB\_\_CLU1B14 EQU 00EH ; Select CLU1B.14

CLU1MX\_MXB\_\_CLU1B15 EQU 00FH ; Select CLU1B.15

CLU1MX\_MXA\_\_FMASK EQU 0F0H ; CLU1 A Input Multiplexer Selection

CLU1MX\_MXA\_\_SHIFT EQU 004H ; CLU1 A Input Multiplexer Selection

CLU1MX\_MXA\_\_CLU1A0 EQU 000H ; Select CLU1A.0

CLU1MX\_MXA\_\_CLU1A1 EQU 010H ; Select CLU1A.1

CLU1MX\_MXA\_\_CLU1A2 EQU 020H ; Select CLU1A.2

CLU1MX\_MXA\_\_CLU1A3 EQU 030H ; Select CLU1A.3

CLU1MX\_MXA\_\_CLU1A4 EQU 040H ; Select CLU1A.4

CLU1MX\_MXA\_\_CLU1A5 EQU 050H ; Select CLU1A.5

CLU1MX\_MXA\_\_CLU1A6 EQU 060H ; Select CLU1A.6

CLU1MX\_MXA\_\_CLU1A7 EQU 070H ; Select CLU1A.7

CLU1MX\_MXA\_\_CLU1A8 EQU 080H ; Select CLU1A.8

CLU1MX\_MXA\_\_CLU1A9 EQU 090H ; Select CLU1A.9

CLU1MX\_MXA\_\_CLU1A10 EQU 0A0H ; Select CLU1A.10

CLU1MX\_MXA\_\_CLU1A11 EQU 0B0H ; Select CLU1A.11

CLU1MX\_MXA\_\_CLU1A12 EQU 0C0H ; Select CLU1A.12

CLU1MX\_MXA\_\_CLU1A13 EQU 0D0H ; Select CLU1A.13

CLU1MX\_MXA\_\_CLU1A14 EQU 0E0H ; Select CLU1A.14

CLU1MX\_MXA\_\_CLU1A15 EQU 0F0H ; Select CLU1A.15

;------------------------------------------------------------------------------

; CLU2CF Enums (Configurable Logic Unit 2 Configuration @ 0xB6)

;------------------------------------------------------------------------------

CLU2CF\_CLKSEL\_\_FMASK EQU 003H ; CLU D flip-flop Clock Selection

CLU2CF\_CLKSEL\_\_SHIFT EQU 000H ; CLU D flip-flop Clock Selection

CLU2CF\_CLKSEL\_\_CARRY\_IN EQU 000H ; The carry-in signal.

CLU2CF\_CLKSEL\_\_MXA\_INPUT EQU 001H ; The MXA input.

CLU2CF\_CLKSEL\_\_SYSCLK EQU 002H ; SYSCLK.

CLU2CF\_CLKSEL\_\_ALTCLK EQU 003H ; The alternate clock signal CLU2ALTCLK.

CLU2CF\_CLKINV\_\_BMASK EQU 004H ; CLU D flip-flop Clock Invert

CLU2CF\_CLKINV\_\_SHIFT EQU 002H ; CLU D flip-flop Clock Invert

CLU2CF\_CLKINV\_\_NORMAL EQU 000H ; Clock signal is not inverted.

CLU2CF\_CLKINV\_\_INVERT EQU 004H ; Clock signal will be inverted.

CLU2CF\_RST\_\_BMASK EQU 008H ; CLU D flip-flop Reset

CLU2CF\_RST\_\_SHIFT EQU 003H ; CLU D flip-flop Reset

CLU2CF\_RST\_\_RESET EQU 008H ; Reset the flip flop.

CLU2CF\_OEN\_\_BMASK EQU 040H ; CLU Port Output Enable

CLU2CF\_OEN\_\_SHIFT EQU 006H ; CLU Port Output Enable

CLU2CF\_OEN\_\_DISABLE EQU 000H ; Disables asynchronous output to the selected GPIO

; pin

CLU2CF\_OEN\_\_ENABLE EQU 040H ; Enables asynchronous output to the selected GPIO

; pin

CLU2CF\_OUTSEL\_\_BMASK EQU 080H ; CLU Output Select

CLU2CF\_OUTSEL\_\_SHIFT EQU 007H ; CLU Output Select

CLU2CF\_OUTSEL\_\_D\_FF EQU 000H ; Select D flip-flop output of CLU

CLU2CF\_OUTSEL\_\_LUT EQU 080H ; Select LUT output.

;------------------------------------------------------------------------------

; CLU2FN Enums (Configurable Logic Unit 2 Function Select @ 0xB5)

;------------------------------------------------------------------------------

CLU2FN\_FNSEL\_\_FMASK EQU 0FFH ; CLU Look-Up-Table function select

CLU2FN\_FNSEL\_\_SHIFT EQU 000H ; CLU Look-Up-Table function select

;------------------------------------------------------------------------------

; CLU2MX Enums (Configurable Logic Unit 2 Multiplexer @ 0x91)

;------------------------------------------------------------------------------

CLU2MX\_MXB\_\_FMASK EQU 00FH ; CLU2 B Input Multiplexer Selection

CLU2MX\_MXB\_\_SHIFT EQU 000H ; CLU2 B Input Multiplexer Selection

CLU2MX\_MXB\_\_CLU2B0 EQU 000H ; Select CLU2B.0

CLU2MX\_MXB\_\_CLU2B1 EQU 001H ; Select CLU2B.1

CLU2MX\_MXB\_\_CLU2B2 EQU 002H ; Select CLU2B.2

CLU2MX\_MXB\_\_CLU2B3 EQU 003H ; Select CLU2B.3

CLU2MX\_MXB\_\_CLU2B4 EQU 004H ; Select CLU2B.4

CLU2MX\_MXB\_\_CLU2B5 EQU 005H ; Select CLU2B.5

CLU2MX\_MXB\_\_CLU2B6 EQU 006H ; Select CLU2B.6

CLU2MX\_MXB\_\_CLU2B7 EQU 007H ; Select CLU2B.7

CLU2MX\_MXB\_\_CLU2B8 EQU 008H ; Select CLU2B.8

CLU2MX\_MXB\_\_CLU2B9 EQU 009H ; Select CLU2B.9

CLU2MX\_MXB\_\_CLU2B10 EQU 00AH ; Select CLU2B.10

CLU2MX\_MXB\_\_CLU2B11 EQU 00BH ; Select CLU2B.11

CLU2MX\_MXB\_\_CLU2B12 EQU 00CH ; Select CLU2B.12

CLU2MX\_MXB\_\_CLU2B13 EQU 00DH ; Select CLU2B.13

CLU2MX\_MXB\_\_CLU2B14 EQU 00EH ; Select CLU2B.14

CLU2MX\_MXB\_\_CLU2B15 EQU 00FH ; Select CLU2B.15

CLU2MX\_MXA\_\_FMASK EQU 0F0H ; CLU2 A Input Multiplexer Selection

CLU2MX\_MXA\_\_SHIFT EQU 004H ; CLU2 A Input Multiplexer Selection

CLU2MX\_MXA\_\_CLU2A0 EQU 000H ; Select CLU2A.0

CLU2MX\_MXA\_\_CLU2A1 EQU 010H ; Select CLU2A.1

CLU2MX\_MXA\_\_CLU2A2 EQU 020H ; Select CLU2A.2

CLU2MX\_MXA\_\_CLU2A3 EQU 030H ; Select CLU2A.3

CLU2MX\_MXA\_\_CLU2A4 EQU 040H ; Select CLU2A.4

CLU2MX\_MXA\_\_CLU2A5 EQU 050H ; Select CLU2A.5

CLU2MX\_MXA\_\_CLU2A6 EQU 060H ; Select CLU2A.6

CLU2MX\_MXA\_\_CLU2A7 EQU 070H ; Select CLU2A.7

CLU2MX\_MXA\_\_CLU2A8 EQU 080H ; Select CLU2A.8

CLU2MX\_MXA\_\_CLU2A9 EQU 090H ; Select CLU2A.9

CLU2MX\_MXA\_\_CLU2A10 EQU 0A0H ; Select CLU2A.10

CLU2MX\_MXA\_\_CLU2A11 EQU 0B0H ; Select CLU2A.11

CLU2MX\_MXA\_\_CLU2A12 EQU 0C0H ; Select CLU2A.12

CLU2MX\_MXA\_\_CLU2A13 EQU 0D0H ; Select CLU2A.13

CLU2MX\_MXA\_\_CLU2A14 EQU 0E0H ; Select CLU2A.14

CLU2MX\_MXA\_\_CLU2A15 EQU 0F0H ; Select CLU2A.15

;------------------------------------------------------------------------------

; CLU3CF Enums (Configurable Logic Unit 3 Configuration @ 0xBF)

;------------------------------------------------------------------------------

CLU3CF\_CLKSEL\_\_FMASK EQU 003H ; CLU D flip-flop Clock Selection

CLU3CF\_CLKSEL\_\_SHIFT EQU 000H ; CLU D flip-flop Clock Selection

CLU3CF\_CLKSEL\_\_CARRY\_IN EQU 000H ; The carry-in signal.

CLU3CF\_CLKSEL\_\_MXA\_INPUT EQU 001H ; The MXA input.

CLU3CF\_CLKSEL\_\_SYSCLK EQU 002H ; SYSCLK.

CLU3CF\_CLKSEL\_\_ALTCLK EQU 003H ; The alternate clock signal CLU3ALTCLK.

CLU3CF\_CLKINV\_\_BMASK EQU 004H ; CLU D flip-flop Clock Invert

CLU3CF\_CLKINV\_\_SHIFT EQU 002H ; CLU D flip-flop Clock Invert

CLU3CF\_CLKINV\_\_NORMAL EQU 000H ; Clock signal is not inverted.

CLU3CF\_CLKINV\_\_INVERT EQU 004H ; Clock signal will be inverted.

CLU3CF\_RST\_\_BMASK EQU 008H ; CLU D flip-flop Reset

CLU3CF\_RST\_\_SHIFT EQU 003H ; CLU D flip-flop Reset

CLU3CF\_RST\_\_RESET EQU 008H ; Reset the flip flop.

CLU3CF\_OEN\_\_BMASK EQU 040H ; CLU Port Output Enable

CLU3CF\_OEN\_\_SHIFT EQU 006H ; CLU Port Output Enable

CLU3CF\_OEN\_\_DISABLE EQU 000H ; Disables asynchronous output to the selected GPIO

; pin

CLU3CF\_OEN\_\_ENABLE EQU 040H ; Enables asynchronous output to the selected GPIO

; pin

CLU3CF\_OUTSEL\_\_BMASK EQU 080H ; CLU Output Select

CLU3CF\_OUTSEL\_\_SHIFT EQU 007H ; CLU Output Select

CLU3CF\_OUTSEL\_\_D\_FF EQU 000H ; Select D flip-flop output of CLU

CLU3CF\_OUTSEL\_\_LUT EQU 080H ; Select LUT output.

;------------------------------------------------------------------------------

; CLU3FN Enums (Configurable Logic Unit 3 Function Select @ 0xBE)

;------------------------------------------------------------------------------

CLU3FN\_FNSEL\_\_FMASK EQU 0FFH ; CLU Look-Up-Table function select

CLU3FN\_FNSEL\_\_SHIFT EQU 000H ; CLU Look-Up-Table function select

;------------------------------------------------------------------------------

; CLU3MX Enums (Configurable Logic Unit 3 Multiplexer @ 0xAE)

;------------------------------------------------------------------------------

CLU3MX\_MXB\_\_FMASK EQU 00FH ; CLU3 B Input Multiplexer Selection

CLU3MX\_MXB\_\_SHIFT EQU 000H ; CLU3 B Input Multiplexer Selection

CLU3MX\_MXB\_\_CLU3B0 EQU 000H ; Select CLU3B.0

CLU3MX\_MXB\_\_CLU3B1 EQU 001H ; Select CLU3B.1

CLU3MX\_MXB\_\_CLU3B2 EQU 002H ; Select CLU3B.2

CLU3MX\_MXB\_\_CLU3B3 EQU 003H ; Select CLU3B.3

CLU3MX\_MXB\_\_CLU3B4 EQU 004H ; Select CLU3B.4

CLU3MX\_MXB\_\_CLU3B5 EQU 005H ; Select CLU3B.5

CLU3MX\_MXB\_\_CLU3B6 EQU 006H ; Select CLU3B.6

CLU3MX\_MXB\_\_CLU3B7 EQU 007H ; Select CLU3B.7

CLU3MX\_MXB\_\_CLU3B8 EQU 008H ; Select CLU3B.8

CLU3MX\_MXB\_\_CLU3B9 EQU 009H ; Select CLU3B.9

CLU3MX\_MXB\_\_CLU3B10 EQU 00AH ; Select CLU3B.10

CLU3MX\_MXB\_\_CLU3B11 EQU 00BH ; Select CLU3B.11

CLU3MX\_MXB\_\_CLU3B12 EQU 00CH ; Select CLU3B.12

CLU3MX\_MXB\_\_CLU3B13 EQU 00DH ; Select CLU3B.13

CLU3MX\_MXB\_\_CLU3B14 EQU 00EH ; Select CLU3B.14

CLU3MX\_MXB\_\_CLU3B15 EQU 00FH ; Select CLU3B.15

CLU3MX\_MXA\_\_FMASK EQU 0F0H ; CLU3 A Input Multiplexer Selection

CLU3MX\_MXA\_\_SHIFT EQU 004H ; CLU3 A Input Multiplexer Selection

CLU3MX\_MXA\_\_CLU3A0 EQU 000H ; Select CLU3A.0

CLU3MX\_MXA\_\_CLU3A1 EQU 010H ; Select CLU3A.1

CLU3MX\_MXA\_\_CLU3A2 EQU 020H ; Select CLU3A.2

CLU3MX\_MXA\_\_CLU3A3 EQU 030H ; Select CLU3A.3

CLU3MX\_MXA\_\_CLU3A4 EQU 040H ; Select CLU3A.4

CLU3MX\_MXA\_\_CLU3A5 EQU 050H ; Select CLU3A.5

CLU3MX\_MXA\_\_CLU3A6 EQU 060H ; Select CLU3A.6

CLU3MX\_MXA\_\_CLU3A7 EQU 070H ; Select CLU3A.7

CLU3MX\_MXA\_\_CLU3A8 EQU 080H ; Select CLU3A.8

CLU3MX\_MXA\_\_CLU3A9 EQU 090H ; Select CLU3A.9

CLU3MX\_MXA\_\_CLU3A10 EQU 0A0H ; Select CLU3A.10

CLU3MX\_MXA\_\_CLU3A11 EQU 0B0H ; Select CLU3A.11

CLU3MX\_MXA\_\_CLU3A12 EQU 0C0H ; Select CLU3A.12

CLU3MX\_MXA\_\_CLU3A13 EQU 0D0H ; Select CLU3A.13

CLU3MX\_MXA\_\_CLU3A14 EQU 0E0H ; Select CLU3A.14

CLU3MX\_MXA\_\_CLU3A15 EQU 0F0H ; Select CLU3A.15

;------------------------------------------------------------------------------

; CLEN0 Enums (Configurable Logic Enable 0 @ 0xC6)

;------------------------------------------------------------------------------

CLEN0\_C0EN\_\_BMASK EQU 001H ; CLU0 Enable

CLEN0\_C0EN\_\_SHIFT EQU 000H ; CLU0 Enable

CLEN0\_C0EN\_\_DISABLE EQU 000H ; CLU0 is disabled. The output of the block will be

; logic low.

CLEN0\_C0EN\_\_ENABLE EQU 001H ; CLU0 is enabled.

CLEN0\_C1EN\_\_BMASK EQU 002H ; CLU1 Enable

CLEN0\_C1EN\_\_SHIFT EQU 001H ; CLU1 Enable

CLEN0\_C1EN\_\_DISABLE EQU 000H ; CLU1 is disabled. The output of the block will be

; logic low.

CLEN0\_C1EN\_\_ENABLE EQU 002H ; CLU1 is enabled.

CLEN0\_C2EN\_\_BMASK EQU 004H ; CLU2 Enable

CLEN0\_C2EN\_\_SHIFT EQU 002H ; CLU2 Enable

CLEN0\_C2EN\_\_DISABLE EQU 000H ; CLU2 is disabled. The output of the block will be

; logic low.

CLEN0\_C2EN\_\_ENABLE EQU 004H ; CLU2 is enabled.

CLEN0\_C3EN\_\_BMASK EQU 008H ; CLU3 Enable

CLEN0\_C3EN\_\_SHIFT EQU 003H ; CLU3 Enable

CLEN0\_C3EN\_\_DISABLE EQU 000H ; CLU3 is disabled. The output of the block will be

; logic low.

CLEN0\_C3EN\_\_ENABLE EQU 008H ; CLU3 is enabled.

;------------------------------------------------------------------------------

; CLIE0 Enums (Configurable Logic Interrupt Enable 0 @ 0xC7)

;------------------------------------------------------------------------------

CLIE0\_C0FIE\_\_BMASK EQU 001H ; CLU0 Falling Edge Interrupt Enable

CLIE0\_C0FIE\_\_SHIFT EQU 000H ; CLU0 Falling Edge Interrupt Enable

CLIE0\_C0FIE\_\_DISABLE EQU 000H ; Interrupts will not be generated for CLU0 falling-

; edge events.

CLIE0\_C0FIE\_\_ENABLE EQU 001H ; Interrupts will be generated for CLU0 falling-edge

; events.

CLIE0\_C0RIE\_\_BMASK EQU 002H ; CLU0 Rising Edge Interrupt Enable

CLIE0\_C0RIE\_\_SHIFT EQU 001H ; CLU0 Rising Edge Interrupt Enable

CLIE0\_C0RIE\_\_DISABLE EQU 000H ; Interrupts will not be generated for CLU0 rising-

; edge events.

CLIE0\_C0RIE\_\_ENABLE EQU 002H ; Interrupts will be generated for CLU0 rising-edge

; events.

CLIE0\_C1FIE\_\_BMASK EQU 004H ; CLU1 Falling Edge Interrupt Enable

CLIE0\_C1FIE\_\_SHIFT EQU 002H ; CLU1 Falling Edge Interrupt Enable

CLIE0\_C1FIE\_\_DISABLE EQU 000H ; Interrupts will not be generated for CLU1 falling-

; edge events.

CLIE0\_C1FIE\_\_ENABLE EQU 004H ; Interrupts will be generated for CLU1 falling-edge

; events.

CLIE0\_C1RIE\_\_BMASK EQU 008H ; CLU1 Rising Edge Interrupt Enable

CLIE0\_C1RIE\_\_SHIFT EQU 003H ; CLU1 Rising Edge Interrupt Enable

CLIE0\_C1RIE\_\_DISABLE EQU 000H ; Interrupts will not be generated for CLU1 rising-

; edge events.

CLIE0\_C1RIE\_\_ENABLE EQU 008H ; Interrupts will be generated for CLU1 rising-edge

; events.

CLIE0\_C2FIE\_\_BMASK EQU 010H ; CLU2 Falling Edge Interrupt Enable

CLIE0\_C2FIE\_\_SHIFT EQU 004H ; CLU2 Falling Edge Interrupt Enable

CLIE0\_C2FIE\_\_DISABLE EQU 000H ; Interrupts will not be generated for CLU2 falling-

; edge events.

CLIE0\_C2FIE\_\_ENABLE EQU 010H ; Interrupts will be generated for CLU2 falling-edge

; events.

CLIE0\_C2RIE\_\_BMASK EQU 020H ; CLU2 Rising Edge Interrupt Enable

CLIE0\_C2RIE\_\_SHIFT EQU 005H ; CLU2 Rising Edge Interrupt Enable

CLIE0\_C2RIE\_\_DISABLE EQU 000H ; Interrupts will not be generated for CLU2 rising-

; edge events.

CLIE0\_C2RIE\_\_ENABLE EQU 020H ; Interrupts will be generated for CLU2 rising-edge

; events.

CLIE0\_C3FIE\_\_BMASK EQU 040H ; CLU3 Falling Edge Interrupt Enable

CLIE0\_C3FIE\_\_SHIFT EQU 006H ; CLU3 Falling Edge Interrupt Enable

CLIE0\_C3FIE\_\_DISABLE EQU 000H ; Interrupts will not be generated for CLU3 falling-

; edge events.

CLIE0\_C3FIE\_\_ENABLE EQU 040H ; Interrupts will be generated for CLU3 falling-edge

; events.

CLIE0\_C3RIE\_\_BMASK EQU 080H ; CLU3 Rising Edge Interrupt Enable

CLIE0\_C3RIE\_\_SHIFT EQU 007H ; CLU3 Rising Edge Interrupt Enable

CLIE0\_C3RIE\_\_DISABLE EQU 000H ; Interrupts will not be generated for CLU3 rising-

; edge events.

CLIE0\_C3RIE\_\_ENABLE EQU 080H ; Interrupts will be generated for CLU3 rising-edge

; events.

;------------------------------------------------------------------------------

; CLIF0 Enums (Configurable Logic Interrupt Flag 0 @ 0xE8)

;------------------------------------------------------------------------------

CLIF0\_C0FIF\_\_BMASK EQU 001H ; CLU0 Falling Edge Interrupt Flag

CLIF0\_C0FIF\_\_SHIFT EQU 000H ; CLU0 Falling Edge Interrupt Flag

CLIF0\_C0FIF\_\_NOT\_SET EQU 000H ; A CLU0 falling edge has not been detected since

; this flag was last cleared.

CLIF0\_C0FIF\_\_SET EQU 001H ; A CLU0 falling edge (synchronized with SYSCLK) has

; occurred. This bit must be cleared by firmware.

CLIF0\_C0RIF\_\_BMASK EQU 002H ; CLU0 Rising Edge Interrupt Flag

CLIF0\_C0RIF\_\_SHIFT EQU 001H ; CLU0 Rising Edge Interrupt Flag

CLIF0\_C0RIF\_\_NOT\_SET EQU 000H ; A CLU0 rising edge has not been detected since

; this flag was last cleared.

CLIF0\_C0RIF\_\_SET EQU 002H ; A CLU0 rising edge (synchronized with SYSCLK) has

; occurred. This bit must be cleared by firmware.

CLIF0\_C1FIF\_\_BMASK EQU 004H ; CLU1 Falling Edge Interrupt Flag

CLIF0\_C1FIF\_\_SHIFT EQU 002H ; CLU1 Falling Edge Interrupt Flag

CLIF0\_C1FIF\_\_NOT\_SET EQU 000H ; A CLU1 falling edge has not been detected since

; this flag was last cleared.

CLIF0\_C1FIF\_\_SET EQU 004H ; A CLU1 falling edge (synchronized with SYSCLK) has

; occurred. This bit must be cleared by firmware.

CLIF0\_C1RIF\_\_BMASK EQU 008H ; CLU1 Rising Edge Interrupt Flag

CLIF0\_C1RIF\_\_SHIFT EQU 003H ; CLU1 Rising Edge Interrupt Flag

CLIF0\_C1RIF\_\_NOT\_SET EQU 000H ; A CLU1 rising edge has not been detected since

; this flag was last cleared.

CLIF0\_C1RIF\_\_SET EQU 008H ; A CLU1 rising edge (synchronized with SYSCLK) has

; occurred. This bit must be cleared by firmware.

CLIF0\_C2FIF\_\_BMASK EQU 010H ; CLU2 Falling Edge Interrupt Flag

CLIF0\_C2FIF\_\_SHIFT EQU 004H ; CLU2 Falling Edge Interrupt Flag

CLIF0\_C2FIF\_\_NOT\_SET EQU 000H ; A CLU2 falling edge has not been detected since

; this flag was last cleared.

CLIF0\_C2FIF\_\_SET EQU 010H ; A CLU2 falling edge (synchronized with SYSCLK) has

; occurred. This bit must be cleared by firmware.

CLIF0\_C2RIF\_\_BMASK EQU 020H ; CLU2 Rising Edge Interrupt Flag

CLIF0\_C2RIF\_\_SHIFT EQU 005H ; CLU2 Rising Edge Interrupt Flag

CLIF0\_C2RIF\_\_NOT\_SET EQU 000H ; A CLU2 rising edge has not been detected since

; this flag was last cleared.

CLIF0\_C2RIF\_\_SET EQU 020H ; A CLU2 rising edge (synchronized with SYSCLK) has

; occurred. This bit must be cleared by firmware.

CLIF0\_C3FIF\_\_BMASK EQU 040H ; CLU3 Falling Edge Interrupt Flag

CLIF0\_C3FIF\_\_SHIFT EQU 006H ; CLU3 Falling Edge Interrupt Flag

CLIF0\_C3FIF\_\_NOT\_SET EQU 000H ; A CLU3 falling edge has not been detected since

; this flag was last cleared.

CLIF0\_C3FIF\_\_SET EQU 040H ; A CLU3 falling edge (synchronized with SYSCLK) has

; occurred. This bit must be cleared by firmware.

CLIF0\_C3RIF\_\_BMASK EQU 080H ; CLU3 Rising Edge Interrupt Flag

CLIF0\_C3RIF\_\_SHIFT EQU 007H ; CLU3 Rising Edge Interrupt Flag

CLIF0\_C3RIF\_\_NOT\_SET EQU 000H ; A CLU3 rising edge has not been detected since

; this flag was last cleared.

CLIF0\_C3RIF\_\_SET EQU 080H ; A CLU3 rising edge (synchronized with SYSCLK) has

; occurred. This bit must be cleared by firmware.

;------------------------------------------------------------------------------

; CLOUT0 Enums (Configurable Logic Output 0 @ 0xD1)

;------------------------------------------------------------------------------

CLOUT0\_C0OUT\_\_BMASK EQU 001H ; CLU0 Output State

CLOUT0\_C0OUT\_\_SHIFT EQU 000H ; CLU0 Output State

CLOUT0\_C1OUT\_\_BMASK EQU 002H ; CLU1 Output State

CLOUT0\_C1OUT\_\_SHIFT EQU 001H ; CLU1 Output State

CLOUT0\_C2OUT\_\_BMASK EQU 004H ; CLU2 Output State

CLOUT0\_C2OUT\_\_SHIFT EQU 002H ; CLU2 Output State

CLOUT0\_C3OUT\_\_BMASK EQU 008H ; CLU3 Output State

CLOUT0\_C3OUT\_\_SHIFT EQU 003H ; CLU3 Output State

;------------------------------------------------------------------------------

; CMP0CN0 Enums (Comparator 0 Control 0 @ 0x9B)

;------------------------------------------------------------------------------

CMP0CN0\_CPHYN\_\_FMASK EQU 003H ; Comparator Negative Hysteresis Control

CMP0CN0\_CPHYN\_\_SHIFT EQU 000H ; Comparator Negative Hysteresis Control

CMP0CN0\_CPHYN\_\_DISABLED EQU 000H ; Negative Hysteresis disabled.

CMP0CN0\_CPHYN\_\_ENABLED\_MODE1 EQU 001H ; Negative Hysteresis = Hysteresis 1.

CMP0CN0\_CPHYN\_\_ENABLED\_MODE2 EQU 002H ; Negative Hysteresis = Hysteresis 2.

CMP0CN0\_CPHYN\_\_ENABLED\_MODE3 EQU 003H ; Negative Hysteresis = Hysteresis 3 (Maximum).

CMP0CN0\_CPHYP\_\_FMASK EQU 00CH ; Comparator Positive Hysteresis Control

CMP0CN0\_CPHYP\_\_SHIFT EQU 002H ; Comparator Positive Hysteresis Control

CMP0CN0\_CPHYP\_\_DISABLED EQU 000H ; Positive Hysteresis disabled.

CMP0CN0\_CPHYP\_\_ENABLED\_MODE1 EQU 004H ; Positive Hysteresis = Hysteresis 1.

CMP0CN0\_CPHYP\_\_ENABLED\_MODE2 EQU 008H ; Positive Hysteresis = Hysteresis 2.

CMP0CN0\_CPHYP\_\_ENABLED\_MODE3 EQU 00CH ; Positive Hysteresis = Hysteresis 3 (Maximum).

CMP0CN0\_CPFIF\_\_BMASK EQU 010H ; Comparator Falling-Edge Flag

CMP0CN0\_CPFIF\_\_SHIFT EQU 004H ; Comparator Falling-Edge Flag

CMP0CN0\_CPFIF\_\_NOT\_SET EQU 000H ; No comparator falling edge has occurred since this

; flag was last cleared.

CMP0CN0\_CPFIF\_\_FALLING\_EDGE EQU 010H ; Comparator falling edge has occurred.

CMP0CN0\_CPRIF\_\_BMASK EQU 020H ; Comparator Rising-Edge Flag

CMP0CN0\_CPRIF\_\_SHIFT EQU 005H ; Comparator Rising-Edge Flag

CMP0CN0\_CPRIF\_\_NOT\_SET EQU 000H ; No comparator rising edge has occurred since this

; flag was last cleared.

CMP0CN0\_CPRIF\_\_RISING\_EDGE EQU 020H ; Comparator rising edge has occurred.

CMP0CN0\_CPOUT\_\_BMASK EQU 040H ; Comparator Output State Flag

CMP0CN0\_CPOUT\_\_SHIFT EQU 006H ; Comparator Output State Flag

CMP0CN0\_CPOUT\_\_POS\_LESS\_THAN\_NEG EQU 000H ; Voltage on CP0P < CP0N.

CMP0CN0\_CPOUT\_\_POS\_GREATER\_THAN\_NEG EQU 040H ; Voltage on CP0P > CP0N.

CMP0CN0\_CPEN\_\_BMASK EQU 080H ; Comparator Enable

CMP0CN0\_CPEN\_\_SHIFT EQU 007H ; Comparator Enable

CMP0CN0\_CPEN\_\_DISABLED EQU 000H ; Comparator disabled.

CMP0CN0\_CPEN\_\_ENABLED EQU 080H ; Comparator enabled.

;------------------------------------------------------------------------------

; CMP0CN1 Enums (Comparator 0 Control 1 @ 0x99)

;------------------------------------------------------------------------------

CMP0CN1\_DACLVL\_\_FMASK EQU 03FH ; Internal Comparator DAC Reference Level

CMP0CN1\_DACLVL\_\_SHIFT EQU 000H ; Internal Comparator DAC Reference Level

CMP0CN1\_CPINH\_\_BMASK EQU 080H ; Output Inhibit

CMP0CN1\_CPINH\_\_SHIFT EQU 007H ; Output Inhibit

CMP0CN1\_CPINH\_\_DISABLED EQU 000H ; The comparator output will always reflect the

; input conditions.

CMP0CN1\_CPINH\_\_ENABLED EQU 080H ; The comparator output will hold state any time the

; PCA CEX2 channel is low.

;------------------------------------------------------------------------------

; CMP0MD Enums (Comparator 0 Mode @ 0x9D)

;------------------------------------------------------------------------------

CMP0MD\_CPMD\_\_FMASK EQU 003H ; Comparator Mode Select

CMP0MD\_CPMD\_\_SHIFT EQU 000H ; Comparator Mode Select

CMP0MD\_CPMD\_\_MODE0 EQU 000H ; Mode 0 (Fastest Response Time, Highest Power

; Consumption)

CMP0MD\_CPMD\_\_MODE1 EQU 001H ; Mode 1

CMP0MD\_CPMD\_\_MODE2 EQU 002H ; Mode 2

CMP0MD\_CPMD\_\_MODE3 EQU 003H ; Mode 3 (Slowest Response Time, Lowest Power

; Consumption)

CMP0MD\_INSL\_\_FMASK EQU 00CH ; Comparator Input Selection

CMP0MD\_INSL\_\_SHIFT EQU 002H ; Comparator Input Selection

CMP0MD\_INSL\_\_CMXP\_CMXN EQU 000H ; Connect the comparator inputs directly to the

; signals selected in the CMP0MX register. CMP+ is

; selected by CMXP and CMP- is selected by CMXN. The

; internal DAC is not active.

CMP0MD\_INSL\_\_CMXP\_GND EQU 004H ; Connect the CMP+ input to the signal selected by

; CMXP, and CMP- is connected to GND. The internal

; DAC is not active.

CMP0MD\_INSL\_\_DAC\_CMXN EQU 008H ; Connect the CMP+ input to the internal DAC output,

; and CMP- is selected by CMXN. The internal DAC

; uses the signal specified by CMXP as its full-

; scale reference.

CMP0MD\_INSL\_\_CMXP\_DAC EQU 00CH ; Connect the CMP- input to the internal DAC output,

; and CMP+ is selected by CMXP. The internal DAC

; uses the signal specified by CMXN as its full-

; scale reference.

CMP0MD\_CPFIE\_\_BMASK EQU 010H ; Comparator Falling-Edge Interrupt Enable

CMP0MD\_CPFIE\_\_SHIFT EQU 004H ; Comparator Falling-Edge Interrupt Enable

CMP0MD\_CPFIE\_\_FALL\_INT\_DISABLED EQU 000H ; Comparator falling-edge interrupt disabled.

CMP0MD\_CPFIE\_\_FALL\_INT\_ENABLED EQU 010H ; Comparator falling-edge interrupt enabled.

CMP0MD\_CPRIE\_\_BMASK EQU 020H ; Comparator Rising-Edge Interrupt Enable

CMP0MD\_CPRIE\_\_SHIFT EQU 005H ; Comparator Rising-Edge Interrupt Enable

CMP0MD\_CPRIE\_\_RISE\_INT\_DISABLED EQU 000H ; Comparator rising-edge interrupt disabled.

CMP0MD\_CPRIE\_\_RISE\_INT\_ENABLED EQU 020H ; Comparator rising-edge interrupt enabled.

CMP0MD\_CPINV\_\_BMASK EQU 040H ; Output Inversion

CMP0MD\_CPINV\_\_SHIFT EQU 006H ; Output Inversion

CMP0MD\_CPINV\_\_NORMAL EQU 000H ; Output is not inverted.

CMP0MD\_CPINV\_\_INVERT EQU 040H ; Output is inverted.

CMP0MD\_CPLOUT\_\_BMASK EQU 080H ; Comparator Latched Output Flag

CMP0MD\_CPLOUT\_\_SHIFT EQU 007H ; Comparator Latched Output Flag

CMP0MD\_CPLOUT\_\_LOW EQU 000H ; Comparator output was logic low at last PCA

; overflow.

CMP0MD\_CPLOUT\_\_HIGH EQU 080H ; Comparator output was logic high at last PCA

; overflow.

;------------------------------------------------------------------------------

; CMP0MX Enums (Comparator 0 Multiplexer Selection @ 0x9F)

;------------------------------------------------------------------------------

CMP0MX\_CMXP\_\_FMASK EQU 00FH ; Comparator Positive Input MUX Selection

CMP0MX\_CMXP\_\_SHIFT EQU 000H ; Comparator Positive Input MUX Selection

CMP0MX\_CMXP\_\_CMP0P0 EQU 000H ; External pin CMP0P.0.

CMP0MX\_CMXP\_\_CMP0P1 EQU 001H ; External pin CMP0P.1.

CMP0MX\_CMXP\_\_CMP0P2 EQU 002H ; External pin CMP0P.2.

CMP0MX\_CMXP\_\_CMP0P3 EQU 003H ; External pin CMP0P.3.

CMP0MX\_CMXP\_\_CMP0P4 EQU 004H ; External pin CMP0P.4.

CMP0MX\_CMXP\_\_CMP0P5 EQU 005H ; External pin CMP0P.5.

CMP0MX\_CMXP\_\_CMP0P6 EQU 006H ; External pin CMP0P.6.

CMP0MX\_CMXP\_\_CMP0P7 EQU 007H ; External pin CMP0P.7.

CMP0MX\_CMXP\_\_CMP0P8 EQU 008H ; External pin CMP0P.8.

CMP0MX\_CMXP\_\_CMP0P9 EQU 009H ; External pin CMP0P.9.

CMP0MX\_CMXP\_\_CMP0P10 EQU 00AH ; External pin CMP0P.10.

CMP0MX\_CMXP\_\_CMP0P11 EQU 00BH ; External pin CMP0P.11.

CMP0MX\_CMXP\_\_CMP0P12 EQU 00CH ; External pin CMP0P.12.

CMP0MX\_CMXP\_\_CMP0P15 EQU 00FH ; External pin CMP0P.15.

CMP0MX\_CMXN\_\_FMASK EQU 0F0H ; Comparator Negative Input MUX Selection

CMP0MX\_CMXN\_\_SHIFT EQU 004H ; Comparator Negative Input MUX Selection

CMP0MX\_CMXN\_\_CMP0N0 EQU 000H ; External pin CMP0N.0.

CMP0MX\_CMXN\_\_CMP0N1 EQU 010H ; External pin CMP0N.1.

CMP0MX\_CMXN\_\_CMP0N2 EQU 020H ; External pin CMP0N.2.

CMP0MX\_CMXN\_\_CMP0N3 EQU 030H ; External pin CMP0N.3.

CMP0MX\_CMXN\_\_CMP0N4 EQU 040H ; External pin CMP0N.4.

CMP0MX\_CMXN\_\_CMP0N5 EQU 050H ; External pin CMP0N.5.

CMP0MX\_CMXN\_\_CMP0N6 EQU 060H ; External pin CMP0N.6.

CMP0MX\_CMXN\_\_CMP0N7 EQU 070H ; External pin CMP0N.7.

CMP0MX\_CMXN\_\_CMP0N8 EQU 080H ; External pin CMP0N.8.

CMP0MX\_CMXN\_\_CMP0N9 EQU 090H ; External pin CMP0N.9.

CMP0MX\_CMXN\_\_CMP0N10 EQU 0A0H ; External pin CMP0N.10.

CMP0MX\_CMXN\_\_CMP0N11 EQU 0B0H ; External pin CMP0N.11.

CMP0MX\_CMXN\_\_CMP0N12 EQU 0C0H ; External pin CMP0N.12.

CMP0MX\_CMXN\_\_CMP0N15 EQU 0F0H ; External pin CMP0N.15.

;------------------------------------------------------------------------------

; CMP1CN0 Enums (Comparator 1 Control 0 @ 0xBF)

;------------------------------------------------------------------------------

CMP1CN0\_CPHYN\_\_FMASK EQU 003H ; Comparator Negative Hysteresis Control

CMP1CN0\_CPHYN\_\_SHIFT EQU 000H ; Comparator Negative Hysteresis Control

CMP1CN0\_CPHYN\_\_DISABLED EQU 000H ; Negative Hysteresis disabled.

CMP1CN0\_CPHYN\_\_ENABLED\_MODE1 EQU 001H ; Negative Hysteresis = Hysteresis 1.

CMP1CN0\_CPHYN\_\_ENABLED\_MODE2 EQU 002H ; Negative Hysteresis = Hysteresis 2.

CMP1CN0\_CPHYN\_\_ENABLED\_MODE3 EQU 003H ; Negative Hysteresis = Hysteresis 3 (Maximum).

CMP1CN0\_CPHYP\_\_FMASK EQU 00CH ; Comparator Positive Hysteresis Control

CMP1CN0\_CPHYP\_\_SHIFT EQU 002H ; Comparator Positive Hysteresis Control

CMP1CN0\_CPHYP\_\_DISABLED EQU 000H ; Positive Hysteresis disabled.

CMP1CN0\_CPHYP\_\_ENABLED\_MODE1 EQU 004H ; Positive Hysteresis = Hysteresis 1.

CMP1CN0\_CPHYP\_\_ENABLED\_MODE2 EQU 008H ; Positive Hysteresis = Hysteresis 2.

CMP1CN0\_CPHYP\_\_ENABLED\_MODE3 EQU 00CH ; Positive Hysteresis = Hysteresis 3 (Maximum).

CMP1CN0\_CPFIF\_\_BMASK EQU 010H ; Comparator Falling-Edge Flag

CMP1CN0\_CPFIF\_\_SHIFT EQU 004H ; Comparator Falling-Edge Flag

CMP1CN0\_CPFIF\_\_NOT\_SET EQU 000H ; No comparator falling edge has occurred since this

; flag was last cleared.

CMP1CN0\_CPFIF\_\_FALLING\_EDGE EQU 010H ; Comparator falling edge has occurred.

CMP1CN0\_CPRIF\_\_BMASK EQU 020H ; Comparator Rising-Edge Flag

CMP1CN0\_CPRIF\_\_SHIFT EQU 005H ; Comparator Rising-Edge Flag

CMP1CN0\_CPRIF\_\_NOT\_SET EQU 000H ; No comparator rising edge has occurred since this

; flag was last cleared.

CMP1CN0\_CPRIF\_\_RISING\_EDGE EQU 020H ; Comparator rising edge has occurred.

CMP1CN0\_CPOUT\_\_BMASK EQU 040H ; Comparator Output State Flag

CMP1CN0\_CPOUT\_\_SHIFT EQU 006H ; Comparator Output State Flag

CMP1CN0\_CPOUT\_\_POS\_LESS\_THAN\_NEG EQU 000H ; Voltage on CP1P < CP1N.

CMP1CN0\_CPOUT\_\_POS\_GREATER\_THAN\_NEG EQU 040H ; Voltage on CP1P > CP1N.

CMP1CN0\_CPEN\_\_BMASK EQU 080H ; Comparator Enable

CMP1CN0\_CPEN\_\_SHIFT EQU 007H ; Comparator Enable

CMP1CN0\_CPEN\_\_DISABLED EQU 000H ; Comparator disabled.

CMP1CN0\_CPEN\_\_ENABLED EQU 080H ; Comparator enabled.

;------------------------------------------------------------------------------

; CMP1CN1 Enums (Comparator 1 Control 1 @ 0xAC)

;------------------------------------------------------------------------------

CMP1CN1\_DACLVL\_\_FMASK EQU 03FH ; Internal Comparator DAC Reference Level

CMP1CN1\_DACLVL\_\_SHIFT EQU 000H ; Internal Comparator DAC Reference Level

CMP1CN1\_CPINH\_\_BMASK EQU 080H ; Output Inhibit

CMP1CN1\_CPINH\_\_SHIFT EQU 007H ; Output Inhibit

CMP1CN1\_CPINH\_\_DISABLED EQU 000H ; The comparator output will always reflect the

; input conditions.

CMP1CN1\_CPINH\_\_ENABLED EQU 080H ; The comparator output will hold state any time the

; PCA CEX2 channel is low.

;------------------------------------------------------------------------------

; CMP1MD Enums (Comparator 1 Mode @ 0xAB)

;------------------------------------------------------------------------------

CMP1MD\_CPMD\_\_FMASK EQU 003H ; Comparator Mode Select

CMP1MD\_CPMD\_\_SHIFT EQU 000H ; Comparator Mode Select

CMP1MD\_CPMD\_\_MODE0 EQU 000H ; Mode 0 (Fastest Response Time, Highest Power

; Consumption)

CMP1MD\_CPMD\_\_MODE1 EQU 001H ; Mode 1

CMP1MD\_CPMD\_\_MODE2 EQU 002H ; Mode 2

CMP1MD\_CPMD\_\_MODE3 EQU 003H ; Mode 3 (Slowest Response Time, Lowest Power

; Consumption)

CMP1MD\_INSL\_\_FMASK EQU 00CH ; Comparator Input Selection

CMP1MD\_INSL\_\_SHIFT EQU 002H ; Comparator Input Selection

CMP1MD\_INSL\_\_CMXP\_CMXN EQU 000H ; Connect the comparator inputs directly to the

; signals selected in the CMP1MX register. CMP+ is

; selected by CMXP and CMP- is selected by CMXN. The

; internal DAC is not active.

CMP1MD\_INSL\_\_CMXP\_GND EQU 004H ; Connect the CMP+ input to the signal selected by

; CMXP, and CMP- is connected to GND. The internal

; DAC is not active.

CMP1MD\_INSL\_\_DAC\_CMXN EQU 008H ; Connect the CMP+ input to the internal DAC output,

; and CMP- is selected by CMXN. The internal DAC

; uses the signal specified by CMXP as its full-

; scale reference.

CMP1MD\_INSL\_\_CMXP\_DAC EQU 00CH ; Connect the CMP- input to the internal DAC output,

; and CMP+ is selected by CMXP. The internal DAC

; uses the signal specified by CMXN as its full-

; scale reference.

CMP1MD\_CPFIE\_\_BMASK EQU 010H ; Comparator Falling-Edge Interrupt Enable

CMP1MD\_CPFIE\_\_SHIFT EQU 004H ; Comparator Falling-Edge Interrupt Enable

CMP1MD\_CPFIE\_\_FALL\_INT\_DISABLED EQU 000H ; Comparator falling-edge interrupt disabled.

CMP1MD\_CPFIE\_\_FALL\_INT\_ENABLED EQU 010H ; Comparator falling-edge interrupt enabled.

CMP1MD\_CPRIE\_\_BMASK EQU 020H ; Comparator Rising-Edge Interrupt Enable

CMP1MD\_CPRIE\_\_SHIFT EQU 005H ; Comparator Rising-Edge Interrupt Enable

CMP1MD\_CPRIE\_\_RISE\_INT\_DISABLED EQU 000H ; Comparator rising-edge interrupt disabled.

CMP1MD\_CPRIE\_\_RISE\_INT\_ENABLED EQU 020H ; Comparator rising-edge interrupt enabled.

CMP1MD\_CPINV\_\_BMASK EQU 040H ; Output Inversion

CMP1MD\_CPINV\_\_SHIFT EQU 006H ; Output Inversion

CMP1MD\_CPINV\_\_NORMAL EQU 000H ; Output is not inverted.

CMP1MD\_CPINV\_\_INVERT EQU 040H ; Output is inverted.

CMP1MD\_CPLOUT\_\_BMASK EQU 080H ; Comparator Latched Output Flag

CMP1MD\_CPLOUT\_\_SHIFT EQU 007H ; Comparator Latched Output Flag

CMP1MD\_CPLOUT\_\_LOW EQU 000H ; Comparator output was logic low at last PCA

; overflow.

CMP1MD\_CPLOUT\_\_HIGH EQU 080H ; Comparator output was logic high at last PCA

; overflow.

;------------------------------------------------------------------------------

; CMP1MX Enums (Comparator 1 Multiplexer Selection @ 0xAA)

;------------------------------------------------------------------------------

CMP1MX\_CMXP\_\_FMASK EQU 00FH ; Comparator Positive Input MUX Selection

CMP1MX\_CMXP\_\_SHIFT EQU 000H ; Comparator Positive Input MUX Selection

CMP1MX\_CMXP\_\_CMP1P0 EQU 000H ; External pin CMP1P.0.

CMP1MX\_CMXP\_\_CMP1P1 EQU 001H ; External pin CMP1P.1.

CMP1MX\_CMXP\_\_CMP1P2 EQU 002H ; External pin CMP1P.2.

CMP1MX\_CMXP\_\_CMP1P3 EQU 003H ; External pin CMP1P.3.

CMP1MX\_CMXP\_\_CMP1P4 EQU 004H ; External pin CMP1P.4.

CMP1MX\_CMXP\_\_CMP1P5 EQU 005H ; External pin CMP1P.5.

CMP1MX\_CMXP\_\_CMP1P6 EQU 006H ; External pin CMP1P.6.

CMP1MX\_CMXP\_\_CMP1P7 EQU 007H ; External pin CMP1P.7.

CMP1MX\_CMXP\_\_CMP1P8 EQU 008H ; External pin CMP1P.8.

CMP1MX\_CMXP\_\_CMP1P9 EQU 009H ; External pin CMP1P.9.

CMP1MX\_CMXP\_\_CMP1P10 EQU 00AH ; External pin CMP1P.10.

CMP1MX\_CMXP\_\_CMP1P11 EQU 00BH ; External pin CMP1P.11.

CMP1MX\_CMXP\_\_CMP1P12 EQU 00CH ; External pin CMP1P.12.

CMP1MX\_CMXP\_\_CMP1P15 EQU 00FH ; External pin CMP1P.15.

CMP1MX\_CMXN\_\_FMASK EQU 0F0H ; Comparator Negative Input MUX Selection

CMP1MX\_CMXN\_\_SHIFT EQU 004H ; Comparator Negative Input MUX Selection

CMP1MX\_CMXN\_\_CMP1N0 EQU 000H ; External pin CMP1N.0.

CMP1MX\_CMXN\_\_CMP1N1 EQU 010H ; External pin CMP1N.1.

CMP1MX\_CMXN\_\_CMP1N2 EQU 020H ; External pin CMP1N.2.

CMP1MX\_CMXN\_\_CMP1N3 EQU 030H ; External pin CMP1N.3.

CMP1MX\_CMXN\_\_CMP1N4 EQU 040H ; External pin CMP1N.4.

CMP1MX\_CMXN\_\_CMP1N5 EQU 050H ; External pin CMP1N.5.

CMP1MX\_CMXN\_\_CMP1N6 EQU 060H ; External pin CMP1N.6.

CMP1MX\_CMXN\_\_CMP1N7 EQU 070H ; External pin CMP1N.7.

CMP1MX\_CMXN\_\_CMP1N8 EQU 080H ; External pin CMP1N.8.

CMP1MX\_CMXN\_\_CMP1N9 EQU 090H ; External pin CMP1N.9.

CMP1MX\_CMXN\_\_CMP1N10 EQU 0A0H ; External pin CMP1N.10.

CMP1MX\_CMXN\_\_CMP1N11 EQU 0B0H ; External pin CMP1N.11.

CMP1MX\_CMXN\_\_CMP1N12 EQU 0C0H ; External pin CMP1N.12.

CMP1MX\_CMXN\_\_CMP1N15 EQU 0F0H ; External pin CMP1N.15.

;------------------------------------------------------------------------------

; CRC0CN0 Enums (CRC0 Control 0 @ 0xCE)

;------------------------------------------------------------------------------

CRC0CN0\_CRCPNT\_\_BMASK EQU 001H ; CRC Result Pointer

CRC0CN0\_CRCPNT\_\_SHIFT EQU 000H ; CRC Result Pointer

CRC0CN0\_CRCPNT\_\_ACCESS\_LOWER EQU 000H ; CRC0DAT accesses bits 7-0 of the 16-bit CRC

; result.

CRC0CN0\_CRCPNT\_\_ACCESS\_UPPER EQU 001H ; CRC0DAT accesses bits 15-8 of the 16-bit CRC

; result.

CRC0CN0\_CRCVAL\_\_BMASK EQU 004H ; CRC Initialization Value

CRC0CN0\_CRCVAL\_\_SHIFT EQU 002H ; CRC Initialization Value

CRC0CN0\_CRCVAL\_\_SET\_ZEROES EQU 000H ; CRC result is set to 0x0000 on write of 1 to

; CRCINIT.

CRC0CN0\_CRCVAL\_\_SET\_ONES EQU 004H ; CRC result is set to 0xFFFF on write of 1 to

; CRCINIT.

CRC0CN0\_CRCINIT\_\_BMASK EQU 008H ; CRC Initialization Enable

CRC0CN0\_CRCINIT\_\_SHIFT EQU 003H ; CRC Initialization Enable

CRC0CN0\_CRCINIT\_\_DO\_NOT\_INIT EQU 000H ; Do not initialize the CRC result.

CRC0CN0\_CRCINIT\_\_INIT EQU 008H ; Initialize the CRC result to ones or zeroes vased

; on the value of CRCVAL.

;------------------------------------------------------------------------------

; CRC0CN1 Enums (CRC0 Control 1 @ 0x86)

;------------------------------------------------------------------------------

CRC0CN1\_CRCDN\_\_BMASK EQU 040H ; Automatic CRC Calculation Complete

CRC0CN1\_CRCDN\_\_SHIFT EQU 006H ; Automatic CRC Calculation Complete

CRC0CN1\_CRCDN\_\_NOT\_SET EQU 000H ; A CRC calculation is in progress.

CRC0CN1\_CRCDN\_\_SET EQU 040H ; A CRC calculation is not in progress.

CRC0CN1\_AUTOEN\_\_BMASK EQU 080H ; Automatic CRC Calculation Enable

CRC0CN1\_AUTOEN\_\_SHIFT EQU 007H ; Automatic CRC Calculation Enable

CRC0CN1\_AUTOEN\_\_DISABLED EQU 000H ; Disable automatic CRC operations on flash.

CRC0CN1\_AUTOEN\_\_ENABLED EQU 080H ; Enable automatic CRC operations on flash.

;------------------------------------------------------------------------------

; CRC0CNT Enums (CRC0 Automatic Flash Sector Count @ 0xD3)

;------------------------------------------------------------------------------

CRC0CNT\_CRCCNT\_\_FMASK EQU 0FFH ; Automatic CRC Calculation Block Count

CRC0CNT\_CRCCNT\_\_SHIFT EQU 000H ; Automatic CRC Calculation Block Count

;------------------------------------------------------------------------------

; CRC0DAT Enums (CRC0 Data Output @ 0xCB)

;------------------------------------------------------------------------------

CRC0DAT\_CRC0DAT\_\_FMASK EQU 0FFH ; CRC Data Output

CRC0DAT\_CRC0DAT\_\_SHIFT EQU 000H ; CRC Data Output

;------------------------------------------------------------------------------

; CRC0FLIP Enums (CRC0 Bit Flip @ 0xCF)

;------------------------------------------------------------------------------

CRC0FLIP\_CRC0FLIP\_\_FMASK EQU 0FFH ; CRC0 Bit Flip

CRC0FLIP\_CRC0FLIP\_\_SHIFT EQU 000H ; CRC0 Bit Flip

;------------------------------------------------------------------------------

; CRC0IN Enums (CRC0 Data Input @ 0xCA)

;------------------------------------------------------------------------------

CRC0IN\_CRC0IN\_\_FMASK EQU 0FFH ; CRC Data Input

CRC0IN\_CRC0IN\_\_SHIFT EQU 000H ; CRC Data Input

;------------------------------------------------------------------------------

; CRC0ST Enums (CRC0 Automatic Flash Sector Start @ 0xD2)

;------------------------------------------------------------------------------

CRC0ST\_CRCST\_\_FMASK EQU 0FFH ; Automatic CRC Calculation Starting Block

CRC0ST\_CRCST\_\_SHIFT EQU 000H ; Automatic CRC Calculation Starting Block

;------------------------------------------------------------------------------

; DACGCF0 Enums (DAC Global Configuration 0 @ 0x88)

;------------------------------------------------------------------------------

DACGCF0\_D1SRC\_\_FMASK EQU 003H ; DAC1 Data Source

DACGCF0\_D1SRC\_\_SHIFT EQU 000H ; DAC1 Data Source

DACGCF0\_D1SRC\_\_DAC1 EQU 000H ; Input = DAC1H:DAC1L.

DACGCF0\_D1SRC\_\_DAC1\_INVERT EQU 001H ; Input = Inverse of DAC1H:DAC1L (one's complement).

DACGCF0\_D1SRC\_\_DAC0 EQU 002H ; Input = DAC0H:DAC0L.

DACGCF0\_D1SRC\_\_DAC0\_INVERT EQU 003H ; Input = Inverse of DAC0H:DAC0L (one's complement).

DACGCF0\_D1AMEN\_\_BMASK EQU 004H ; DAC1 Alternating Mode Enable

DACGCF0\_D1AMEN\_\_SHIFT EQU 002H ; DAC1 Alternating Mode Enable

DACGCF0\_D1AMEN\_\_NORMAL EQU 000H ; DAC1 always updates from the data source selected

; in D1SRC. This mode may be used with any trigger

; source.

DACGCF0\_D1AMEN\_\_ALTERNATE EQU 004H ; DAC1 updates occur on the rising or falling edge

; of the trigger signal. On a falling edge, DAC1

; receives the DAC1H/L registers. On a rising edge,

; DAC1 receives the data source selected in D1SRC.

; \*This mode may only be used with Configurable

; Logic trigger sources, and the selected trigger

; source must be high or low for two or more SYSCLK

; cycles.\*

DACGCF0\_D01REFSL\_\_BMASK EQU 008H ; DAC0 and DAC1 Reference Voltage Select

DACGCF0\_D01REFSL\_\_SHIFT EQU 003H ; DAC0 and DAC1 Reference Voltage Select

DACGCF0\_D01REFSL\_\_VREF EQU 000H ; Select the VREF pin.

DACGCF0\_D01REFSL\_\_VDD EQU 008H ; Select the VDD supply.

DACGCF0\_D3SRC\_\_FMASK EQU 030H ; DAC3 Data Source

DACGCF0\_D3SRC\_\_SHIFT EQU 004H ; DAC3 Data Source

DACGCF0\_D3SRC\_\_DAC3 EQU 000H ; Input = DAC3H:DAC3L.

DACGCF0\_D3SRC\_\_DAC3\_INVERT EQU 010H ; Input = Inverse of DAC3H:DAC3L (one's complement).

DACGCF0\_D3SRC\_\_DAC2 EQU 020H ; Input = DAC2H:DAC2L.

DACGCF0\_D3SRC\_\_DAC2\_INVERT EQU 030H ; Input = Inverse of DAC2H:DAC2L (one's complement).

DACGCF0\_D3AMEN\_\_BMASK EQU 040H ; DAC3 Alternating Mode Enable

DACGCF0\_D3AMEN\_\_SHIFT EQU 006H ; DAC3 Alternating Mode Enable

DACGCF0\_D3AMEN\_\_NORMAL EQU 000H ; DAC3 always updates from the data source selected

; in D3SRC. This mode may be used with any trigger

; source.

DACGCF0\_D3AMEN\_\_ALTERNATE EQU 040H ; DAC3 updates occur on the rising or falling edge

; of the trigger signal. On a falling edge, DAC3

; receives the DAC3H/L registers. On a rising edge,

; DAC3 receives the data source selected in D3SRC.

; \*This mode may only be used with Configurable

; Logic trigger sources, and the selected trigger

; source must be high or low for two or more SYSCLK

; cycles.\*

DACGCF0\_D23REFSL\_\_BMASK EQU 080H ; DAC2 and DAC3 Reference Voltage Select

DACGCF0\_D23REFSL\_\_SHIFT EQU 007H ; DAC2 and DAC3 Reference Voltage Select

DACGCF0\_D23REFSL\_\_VREF EQU 000H ; Select the VREF pin.

DACGCF0\_D23REFSL\_\_VDD EQU 080H ; Select the VDD supply.

;------------------------------------------------------------------------------

; DACGCF1 Enums (DAC Global Configuration 1 @ 0x98)

;------------------------------------------------------------------------------

DACGCF1\_D0UDIS\_\_BMASK EQU 001H ; DAC0 Update Disable

DACGCF1\_D0UDIS\_\_SHIFT EQU 000H ; DAC0 Update Disable

DACGCF1\_D0UDIS\_\_ENABLE EQU 000H ; Allow triggers to update DAC0 output.

DACGCF1\_D0UDIS\_\_DISABLE EQU 001H ; Triggers will not update DAC0 output.

DACGCF1\_D1UDIS\_\_BMASK EQU 002H ; DAC1 Update Disable

DACGCF1\_D1UDIS\_\_SHIFT EQU 001H ; DAC1 Update Disable

DACGCF1\_D1UDIS\_\_ENABLE EQU 000H ; Allow triggers to update DAC1 output.

DACGCF1\_D1UDIS\_\_DISABLE EQU 002H ; Triggers will not update DAC1 output.

DACGCF1\_D2UDIS\_\_BMASK EQU 004H ; DAC2 Update Disable

DACGCF1\_D2UDIS\_\_SHIFT EQU 002H ; DAC2 Update Disable

DACGCF1\_D2UDIS\_\_ENABLE EQU 000H ; Allow triggers to update DAC2 output.

DACGCF1\_D2UDIS\_\_DISABLE EQU 004H ; Triggers will not update DAC2 output.

DACGCF1\_D3UDIS\_\_BMASK EQU 008H ; DAC3 Update Disable

DACGCF1\_D3UDIS\_\_SHIFT EQU 003H ; DAC3 Update Disable

DACGCF1\_D3UDIS\_\_ENABLE EQU 000H ; Allow triggers to update DAC3 output.

DACGCF1\_D3UDIS\_\_DISABLE EQU 008H ; Triggers will not update DAC3 output.

;------------------------------------------------------------------------------

; DACGCF2 Enums (DAC Global Configuration 2 @ 0xA2)

;------------------------------------------------------------------------------

DACGCF2\_D01REFGN\_\_FMASK EQU 003H ; DAC0/1 Reference Buffer Gain

DACGCF2\_D01REFGN\_\_SHIFT EQU 000H ; DAC0/1 Reference Buffer Gain

DACGCF2\_D01REFGN\_\_ATTEN\_2P0 EQU 000H ; Selected reference will be attenuated by a factor

; of 2.

DACGCF2\_D01REFGN\_\_ATTEN\_2P4 EQU 001H ; Selected reference will be attenuated by a factor

; of 2.4 (Gain = 1/2.4).

DACGCF2\_D01REFGN\_\_ATTEN\_3P0 EQU 002H ; Selected reference will be attenuated by a factor

; of 3 (Gain = 1/3).

DACGCF2\_D23REFGN\_\_FMASK EQU 030H ; DAC2/3 Reference Buffer Gain

DACGCF2\_D23REFGN\_\_SHIFT EQU 004H ; DAC2/3 Reference Buffer Gain

DACGCF2\_D23REFGN\_\_ATTEN\_2P0 EQU 000H ; Selected reference will be attenuated by a factor

; of 2.

DACGCF2\_D23REFGN\_\_ATTEN\_2P4 EQU 010H ; Selected reference will be attenuated by a factor

; of 2.4 (Gain = 1/2.4).

DACGCF2\_D23REFGN\_\_ATTEN\_3P0 EQU 020H ; Selected reference will be attenuated by a factor

; of 3 (Gain = 1/3).

;------------------------------------------------------------------------------

; DAC0CF0 Enums (DAC0 Configuration 0 @ 0x91)

;------------------------------------------------------------------------------

DAC0CF0\_UPDATE\_\_FMASK EQU 007H ; DAC0 Update Trigger Source

DAC0CF0\_UPDATE\_\_SHIFT EQU 000H ; DAC0 Update Trigger Source

DAC0CF0\_UPDATE\_\_SYSCLK EQU 000H ; DAC0 output updates occur on every clock cycle.

DAC0CF0\_UPDATE\_\_TIMER3 EQU 001H ; DAC0 output updates occur on Timer 3 high byte

; overflow.

DAC0CF0\_UPDATE\_\_TIMER4 EQU 002H ; DAC0 output updates occur on Timer 4 high byte

; overflow.

DAC0CF0\_UPDATE\_\_TIMER5 EQU 003H ; DAC0 output updates occur on Timer 5 high byte

; overflow.

DAC0CF0\_UPDATE\_\_CLU0 EQU 004H ; DAC0 output updates occur on Configurable Logic

; output 0 rising edge.

DAC0CF0\_UPDATE\_\_CLU1 EQU 005H ; DAC0 output updates occur on Configurable Logic

; output 1 rising edge.

DAC0CF0\_UPDATE\_\_CLU2 EQU 006H ; DAC0 output updates occur on Configurable Logic

; output 2 rising edge.

DAC0CF0\_UPDATE\_\_CLU3 EQU 007H ; DAC0 output updates occur on Configurable Logic

; output 3 rising edge.

DAC0CF0\_LJST\_\_BMASK EQU 020H ; DAC0 Left Justify Enable

DAC0CF0\_LJST\_\_SHIFT EQU 005H ; DAC0 Left Justify Enable

DAC0CF0\_LJST\_\_RIGHT\_JUSTIFY EQU 000H ; DAC0 input is treated as right-justified.

DAC0CF0\_LJST\_\_LEFT\_JUSTIFY EQU 020H ; DAC0 input is treated as left-justified.

DAC0CF0\_RSTMD\_\_BMASK EQU 040H ; DAC0 Reset Mode

DAC0CF0\_RSTMD\_\_SHIFT EQU 006H ; DAC0 Reset Mode

DAC0CF0\_RSTMD\_\_NORMAL EQU 000H ; All resets will reset DAC0 and its associated

; registers.

DAC0CF0\_RSTMD\_\_PERSIST EQU 040H ; DAC0 output will persist through all resets except

; for power-on-resets.

DAC0CF0\_EN\_\_BMASK EQU 080H ; DAC0 Enable

DAC0CF0\_EN\_\_SHIFT EQU 007H ; DAC0 Enable

DAC0CF0\_EN\_\_DISABLE EQU 000H ; DAC0 is disabled and not driven at the output pin.

DAC0CF0\_EN\_\_ENABLE EQU 080H ; DAC0 is enabled and will drive the output pin.

;------------------------------------------------------------------------------

; DAC0CF1 Enums (DAC0 Configuration 1 @ 0x92)

;------------------------------------------------------------------------------

DAC0CF1\_DRVGAIN\_\_FMASK EQU 003H ; DAC0 Output Buffer Gain

DAC0CF1\_DRVGAIN\_\_SHIFT EQU 000H ; DAC0 Output Buffer Gain

DAC0CF1\_DRVGAIN\_\_GAIN\_2P0 EQU 000H ; DAC output gain is 2.

DAC0CF1\_DRVGAIN\_\_GAIN\_2P4 EQU 001H ; DAC output gain is 2.4.

DAC0CF1\_DRVGAIN\_\_GAIN\_3P0 EQU 002H ; DAC output gain is 3.

;------------------------------------------------------------------------------

; DAC0H Enums (DAC0 Data Word High Byte @ 0x85)

;------------------------------------------------------------------------------

DAC0H\_DAC0H\_\_FMASK EQU 0FFH ; Data Word High Byte

DAC0H\_DAC0H\_\_SHIFT EQU 000H ; Data Word High Byte

;------------------------------------------------------------------------------

; DAC0L Enums (DAC0 Data Word Low Byte @ 0x84)

;------------------------------------------------------------------------------

DAC0L\_DAC0L\_\_FMASK EQU 0FFH ; Data Word Low Byte

DAC0L\_DAC0L\_\_SHIFT EQU 000H ; Data Word Low Byte

;------------------------------------------------------------------------------

; DAC1CF0 Enums (DAC1 Configuration 0 @ 0x93)

;------------------------------------------------------------------------------

DAC1CF0\_UPDATE\_\_FMASK EQU 007H ; DAC1 Update Trigger Source

DAC1CF0\_UPDATE\_\_SHIFT EQU 000H ; DAC1 Update Trigger Source

DAC1CF0\_UPDATE\_\_SYSCLK EQU 000H ; DAC1 output updates occur on every clock cycle.

DAC1CF0\_UPDATE\_\_TIMER3 EQU 001H ; DAC1 output updates occur on Timer 3 high byte

; overflow.

DAC1CF0\_UPDATE\_\_TIMER4 EQU 002H ; DAC1 output updates occur on Timer 4 high byte

; overflow.

DAC1CF0\_UPDATE\_\_TIMER5 EQU 003H ; DAC1 output updates occur on Timer 5 high byte

; overflow.

DAC1CF0\_UPDATE\_\_CLU0 EQU 004H ; DAC1 output updates occur on Configurable Logic

; output 0 rising edge.

DAC1CF0\_UPDATE\_\_CLU1 EQU 005H ; DAC1 output updates occur on Configurable Logic

; output 1 rising edge.

DAC1CF0\_UPDATE\_\_CLU2 EQU 006H ; DAC1 output updates occur on Configurable Logic

; output 2 rising edge.

DAC1CF0\_UPDATE\_\_CLU3 EQU 007H ; DAC1 output updates occur on Configurable Logic

; output 3 rising edge.

DAC1CF0\_LJST\_\_BMASK EQU 020H ; DAC1 Left Justify Enable

DAC1CF0\_LJST\_\_SHIFT EQU 005H ; DAC1 Left Justify Enable

DAC1CF0\_LJST\_\_RIGHT\_JUSTIFY EQU 000H ; DAC1 input is treated as right-justified.

DAC1CF0\_LJST\_\_LEFT\_JUSTIFY EQU 020H ; DAC1 input is treated as left-justified.

DAC1CF0\_RSTMD\_\_BMASK EQU 040H ; DAC1 Reset Mode

DAC1CF0\_RSTMD\_\_SHIFT EQU 006H ; DAC1 Reset Mode

DAC1CF0\_RSTMD\_\_NORMAL EQU 000H ; All resets will reset DAC1 and its associated

; registers.

DAC1CF0\_RSTMD\_\_PERSIST EQU 040H ; DAC1 output will persist through all resets except

; for power-on-resets.

DAC1CF0\_EN\_\_BMASK EQU 080H ; DAC1 Enable

DAC1CF0\_EN\_\_SHIFT EQU 007H ; DAC1 Enable

DAC1CF0\_EN\_\_DISABLE EQU 000H ; DAC1 is disabled and not driven at the output pin.

DAC1CF0\_EN\_\_ENABLE EQU 080H ; DAC1 is enabled and will drive the output pin.

;------------------------------------------------------------------------------

; DAC1CF1 Enums (DAC1 Configuration 1 @ 0x94)

;------------------------------------------------------------------------------

DAC1CF1\_DRVGAIN\_\_FMASK EQU 003H ; DAC1 Output Buffer Gain

DAC1CF1\_DRVGAIN\_\_SHIFT EQU 000H ; DAC1 Output Buffer Gain

DAC1CF1\_DRVGAIN\_\_GAIN\_2P0 EQU 000H ; DAC output gain is 2.

DAC1CF1\_DRVGAIN\_\_GAIN\_2P4 EQU 001H ; DAC output gain is 2.4.

DAC1CF1\_DRVGAIN\_\_GAIN\_3P0 EQU 002H ; DAC output gain is 3.

;------------------------------------------------------------------------------

; DAC1H Enums (DAC1 Data Word High Byte @ 0x8A)

;------------------------------------------------------------------------------

DAC1H\_DAC1H\_\_FMASK EQU 0FFH ; Data Word High Byte

DAC1H\_DAC1H\_\_SHIFT EQU 000H ; Data Word High Byte

;------------------------------------------------------------------------------

; DAC1L Enums (DAC1 Data Word Low Byte @ 0x89)

;------------------------------------------------------------------------------

DAC1L\_DAC1L\_\_FMASK EQU 0FFH ; Data Word Low Byte

DAC1L\_DAC1L\_\_SHIFT EQU 000H ; Data Word Low Byte

;------------------------------------------------------------------------------

; DAC2CF0 Enums (DAC2 Configuration 0 @ 0x95)

;------------------------------------------------------------------------------

DAC2CF0\_UPDATE\_\_FMASK EQU 007H ; DAC2 Update Trigger Source

DAC2CF0\_UPDATE\_\_SHIFT EQU 000H ; DAC2 Update Trigger Source

DAC2CF0\_UPDATE\_\_SYSCLK EQU 000H ; DAC2 output updates occur on every clock cycle.

DAC2CF0\_UPDATE\_\_TIMER3 EQU 001H ; DAC2 output updates occur on Timer 3 high byte

; overflow.

DAC2CF0\_UPDATE\_\_TIMER4 EQU 002H ; DAC2 output updates occur on Timer 4 high byte

; overflow.

DAC2CF0\_UPDATE\_\_TIMER5 EQU 003H ; DAC2 output updates occur on Timer 5 high byte

; overflow.

DAC2CF0\_UPDATE\_\_CLU0 EQU 004H ; DAC2 output updates occur on Configurable Logic

; output 0 rising edge.

DAC2CF0\_UPDATE\_\_CLU1 EQU 005H ; DAC2 output updates occur on Configurable Logic

; output 1 rising edge.

DAC2CF0\_UPDATE\_\_CLU2 EQU 006H ; DAC2 output updates occur on Configurable Logic

; output 2 rising edge.

DAC2CF0\_UPDATE\_\_CLU3 EQU 007H ; DAC2 output updates occur on Configurable Logic

; output 3 rising edge.

DAC2CF0\_LJST\_\_BMASK EQU 020H ; DAC2 Left Justify Enable

DAC2CF0\_LJST\_\_SHIFT EQU 005H ; DAC2 Left Justify Enable

DAC2CF0\_LJST\_\_RIGHT\_JUSTIFY EQU 000H ; DAC2 input is treated as right-justified.

DAC2CF0\_LJST\_\_LEFT\_JUSTIFY EQU 020H ; DAC2 input is treated as left-justified.

DAC2CF0\_RSTMD\_\_BMASK EQU 040H ; DAC2 Reset Mode

DAC2CF0\_RSTMD\_\_SHIFT EQU 006H ; DAC2 Reset Mode

DAC2CF0\_RSTMD\_\_NORMAL EQU 000H ; All resets will reset DAC2 and its associated

; registers.

DAC2CF0\_RSTMD\_\_PERSIST EQU 040H ; DAC2 output will persist through all resets except

; for power-on-resets.

DAC2CF0\_EN\_\_BMASK EQU 080H ; DAC2 Enable

DAC2CF0\_EN\_\_SHIFT EQU 007H ; DAC2 Enable

DAC2CF0\_EN\_\_DISABLE EQU 000H ; DAC2 is disabled and not driven at the output pin.

DAC2CF0\_EN\_\_ENABLE EQU 080H ; DAC2 is enabled and will drive the output pin.

;------------------------------------------------------------------------------

; DAC2CF1 Enums (DAC2 Configuration 1 @ 0x96)

;------------------------------------------------------------------------------

DAC2CF1\_DRVGAIN\_\_FMASK EQU 003H ; DAC2 Output Buffer Gain

DAC2CF1\_DRVGAIN\_\_SHIFT EQU 000H ; DAC2 Output Buffer Gain

DAC2CF1\_DRVGAIN\_\_GAIN\_2P0 EQU 000H ; DAC output gain is 2.

DAC2CF1\_DRVGAIN\_\_GAIN\_2P4 EQU 001H ; DAC output gain is 2.4.

DAC2CF1\_DRVGAIN\_\_GAIN\_3P0 EQU 002H ; DAC output gain is 3.

;------------------------------------------------------------------------------

; DAC2H Enums (DAC2 Data Word High Byte @ 0x8C)

;------------------------------------------------------------------------------

DAC2H\_DAC2H\_\_FMASK EQU 0FFH ; Data Word High Byte

DAC2H\_DAC2H\_\_SHIFT EQU 000H ; Data Word High Byte

;------------------------------------------------------------------------------

; DAC2L Enums (DAC2 Data Word Low Byte @ 0x8B)

;------------------------------------------------------------------------------

DAC2L\_DAC2L\_\_FMASK EQU 0FFH ; Data Word Low Byte

DAC2L\_DAC2L\_\_SHIFT EQU 000H ; Data Word Low Byte

;------------------------------------------------------------------------------

; DAC3CF0 Enums (DAC3 Configuration 0 @ 0x9A)

;------------------------------------------------------------------------------

DAC3CF0\_UPDATE\_\_FMASK EQU 007H ; DAC3 Update Trigger Source

DAC3CF0\_UPDATE\_\_SHIFT EQU 000H ; DAC3 Update Trigger Source

DAC3CF0\_UPDATE\_\_SYSCLK EQU 000H ; DAC3 output updates occur on every clock cycle.

DAC3CF0\_UPDATE\_\_TIMER3 EQU 001H ; DAC3 output updates occur on Timer 3 high byte

; overflow.

DAC3CF0\_UPDATE\_\_TIMER4 EQU 002H ; DAC3 output updates occur on Timer 4 high byte

; overflow.

DAC3CF0\_UPDATE\_\_TIMER5 EQU 003H ; DAC3 output updates occur on Timer 5 high byte

; overflow.

DAC3CF0\_UPDATE\_\_CLU0 EQU 004H ; DAC3 output updates occur on Configurable Logic

; output 0 rising edge.

DAC3CF0\_UPDATE\_\_CLU1 EQU 005H ; DAC3 output updates occur on Configurable Logic

; output 1 rising edge.

DAC3CF0\_UPDATE\_\_CLU2 EQU 006H ; DAC3 output updates occur on Configurable Logic

; output 2 rising edge.

DAC3CF0\_UPDATE\_\_CLU3 EQU 007H ; DAC3 output updates occur on Configurable Logic

; output 3 rising edge.

DAC3CF0\_LJST\_\_BMASK EQU 020H ; DAC3 Left Justify Enable

DAC3CF0\_LJST\_\_SHIFT EQU 005H ; DAC3 Left Justify Enable

DAC3CF0\_LJST\_\_RIGHT\_JUSTIFY EQU 000H ; DAC3 input is treated as right-justified.

DAC3CF0\_LJST\_\_LEFT\_JUSTIFY EQU 020H ; DAC3 input is treated as left-justified.

DAC3CF0\_RSTMD\_\_BMASK EQU 040H ; DAC3 Reset Mode

DAC3CF0\_RSTMD\_\_SHIFT EQU 006H ; DAC3 Reset Mode

DAC3CF0\_RSTMD\_\_NORMAL EQU 000H ; All resets will reset DAC3 and its associated

; registers.

DAC3CF0\_RSTMD\_\_PERSIST EQU 040H ; DAC3 output will persist through all resets except

; for power-on-resets.

DAC3CF0\_EN\_\_BMASK EQU 080H ; DAC3 Enable

DAC3CF0\_EN\_\_SHIFT EQU 007H ; DAC3 Enable

DAC3CF0\_EN\_\_DISABLE EQU 000H ; DAC3 is disabled and not driven at the output pin.

DAC3CF0\_EN\_\_ENABLE EQU 080H ; DAC3 is enabled and will drive the output pin.

;------------------------------------------------------------------------------

; DAC3CF1 Enums (DAC3 Configuration 1 @ 0x9C)

;------------------------------------------------------------------------------

DAC3CF1\_DRVGAIN\_\_FMASK EQU 003H ; DAC3 Output Buffer Gain

DAC3CF1\_DRVGAIN\_\_SHIFT EQU 000H ; DAC3 Output Buffer Gain

DAC3CF1\_DRVGAIN\_\_GAIN\_2P0 EQU 000H ; DAC output gain is 2.

DAC3CF1\_DRVGAIN\_\_GAIN\_2P4 EQU 001H ; DAC output gain is 2.4.

DAC3CF1\_DRVGAIN\_\_GAIN\_3P0 EQU 002H ; DAC output gain is 3.

;------------------------------------------------------------------------------

; DAC3H Enums (DAC3 Data Word High Byte @ 0x8E)

;------------------------------------------------------------------------------

DAC3H\_DAC3H\_\_FMASK EQU 0FFH ; Data Word High Byte

DAC3H\_DAC3H\_\_SHIFT EQU 000H ; Data Word High Byte

;------------------------------------------------------------------------------

; DAC3L Enums (DAC3 Data Word Low Byte @ 0x8D)

;------------------------------------------------------------------------------

DAC3L\_DAC3L\_\_FMASK EQU 0FFH ; Data Word Low Byte

DAC3L\_DAC3L\_\_SHIFT EQU 000H ; Data Word Low Byte

;------------------------------------------------------------------------------

; DERIVID Enums (Derivative Identification @ 0xAD)

;------------------------------------------------------------------------------

DERIVID\_DERIVID\_\_FMASK EQU 0FFH ; Derivative ID

DERIVID\_DERIVID\_\_SHIFT EQU 000H ; Derivative ID

DERIVID\_DERIVID\_\_EFM8BB31F64G\_QFN32 EQU 001H ; EFM8BB31F64G-{R}-QFN32

DERIVID\_DERIVID\_\_EFM8BB31F64G\_QFP32 EQU 002H ; EFM8BB31F64G-{R}-QFP32

DERIVID\_DERIVID\_\_EFM8BB31F64G\_QSOP24 EQU 003H ; EFM8BB31F64G-{R}-QSOP24

DERIVID\_DERIVID\_\_EFM8BB31F64G\_QFN24 EQU 004H ; EFM8BB31F64G-{R}-QFN24

DERIVID\_DERIVID\_\_EFM8BB31F32G\_QFN32 EQU 005H ; EFM8BB31F32G-{R}-QFN32

DERIVID\_DERIVID\_\_EFM8BB31F32G\_QFP32 EQU 006H ; EFM8BB31F32G-{R}-QFP32

DERIVID\_DERIVID\_\_EFM8BB31F32G\_QSOP24 EQU 007H ; EFM8BB31F32G-{R}-QSOP24

DERIVID\_DERIVID\_\_EFM8BB31F32G\_QFN24 EQU 008H ; EFM8BB31F32G-{R}-QFN24

DERIVID\_DERIVID\_\_EFM8BB31F16G\_QFN32 EQU 009H ; EFM8BB31F16G-{R}-QFN32

DERIVID\_DERIVID\_\_EFM8BB31F16G\_QFP32 EQU 00AH ; EFM8BB31F16G-{R}-QFP32

DERIVID\_DERIVID\_\_EFM8BB31F16G\_QSOP24 EQU 00BH ; EFM8BB31F16G-{R}-QSOP24

;------------------------------------------------------------------------------

; DEVICEID Enums (Device Identification @ 0xB5)

;------------------------------------------------------------------------------

DEVICEID\_DEVICEID\_\_FMASK EQU 0FFH ; Device ID

DEVICEID\_DEVICEID\_\_SHIFT EQU 000H ; Device ID

;------------------------------------------------------------------------------

; REVID Enums (Revision Identifcation @ 0xB6)

;------------------------------------------------------------------------------

REVID\_REVID\_\_FMASK EQU 0FFH ; Revision ID

REVID\_REVID\_\_SHIFT EQU 000H ; Revision ID

REVID\_REVID\_\_REV\_A EQU 000H ; Revision A.

;------------------------------------------------------------------------------

; IT01CF Enums (INT0/INT1 Configuration @ 0xE4)

;------------------------------------------------------------------------------

IT01CF\_IN0SL\_\_FMASK EQU 007H ; INT0 Port Pin Selection

IT01CF\_IN0SL\_\_SHIFT EQU 000H ; INT0 Port Pin Selection

IT01CF\_IN0SL\_\_P0\_0 EQU 000H ; Select P0.0.

IT01CF\_IN0SL\_\_P0\_1 EQU 001H ; Select P0.1.

IT01CF\_IN0SL\_\_P0\_2 EQU 002H ; Select P0.2.

IT01CF\_IN0SL\_\_P0\_3 EQU 003H ; Select P0.3.

IT01CF\_IN0SL\_\_P0\_4 EQU 004H ; Select P0.4.

IT01CF\_IN0SL\_\_P0\_5 EQU 005H ; Select P0.5.

IT01CF\_IN0SL\_\_P0\_6 EQU 006H ; Select P0.6.

IT01CF\_IN0SL\_\_P0\_7 EQU 007H ; Select P0.7.

IT01CF\_IN0PL\_\_BMASK EQU 008H ; INT0 Polarity

IT01CF\_IN0PL\_\_SHIFT EQU 003H ; INT0 Polarity

IT01CF\_IN0PL\_\_ACTIVE\_LOW EQU 000H ; INT0 input is active low.

IT01CF\_IN0PL\_\_ACTIVE\_HIGH EQU 008H ; INT0 input is active high.

IT01CF\_IN1SL\_\_FMASK EQU 070H ; INT1 Port Pin Selection

IT01CF\_IN1SL\_\_SHIFT EQU 004H ; INT1 Port Pin Selection

IT01CF\_IN1SL\_\_P0\_0 EQU 000H ; Select P0.0.

IT01CF\_IN1SL\_\_P0\_1 EQU 010H ; Select P0.1.

IT01CF\_IN1SL\_\_P0\_2 EQU 020H ; Select P0.2.

IT01CF\_IN1SL\_\_P0\_3 EQU 030H ; Select P0.3.

IT01CF\_IN1SL\_\_P0\_4 EQU 040H ; Select P0.4.

IT01CF\_IN1SL\_\_P0\_5 EQU 050H ; Select P0.5.

IT01CF\_IN1SL\_\_P0\_6 EQU 060H ; Select P0.6.

IT01CF\_IN1SL\_\_P0\_7 EQU 070H ; Select P0.7.

IT01CF\_IN1PL\_\_BMASK EQU 080H ; INT1 Polarity

IT01CF\_IN1PL\_\_SHIFT EQU 007H ; INT1 Polarity

IT01CF\_IN1PL\_\_ACTIVE\_LOW EQU 000H ; INT1 input is active low.

IT01CF\_IN1PL\_\_ACTIVE\_HIGH EQU 080H ; INT1 input is active high.

;------------------------------------------------------------------------------

; XOSC0CN Enums (External Oscillator Control @ 0x86)

;------------------------------------------------------------------------------

XOSC0CN\_XFCN\_\_FMASK EQU 007H ; External Oscillator Frequency Control

XOSC0CN\_XFCN\_\_SHIFT EQU 000H ; External Oscillator Frequency Control

XOSC0CN\_XFCN\_\_MODE0 EQU 000H ; Select external oscillator mode 0: Crystal

; frequency <= 20 kHz, RC/C frequency <= 25 kHz.

XOSC0CN\_XFCN\_\_MODE1 EQU 001H ; Select external oscillator mode 1: 20 kHz <

; Crystal frequency <= 58 kHz, 25 kHz < RC/C

; frequency <= 50 kHz.

XOSC0CN\_XFCN\_\_MODE2 EQU 002H ; Select external oscillator mode 2: 58 kHz <

; Crystal frequency <= 155 kHz, 50 kHz < RC/C

; frequency <= 100 kHz.

XOSC0CN\_XFCN\_\_MODE3 EQU 003H ; Select external oscillator mode 3: 155 kHz <

; Crystal frequency <= 415 kHz, 100 kHz < RC/C

; frequency <= 200 kHz.

XOSC0CN\_XFCN\_\_MODE4 EQU 004H ; Select external oscillator mode 4: 415 kHz <

; Crystal frequency <= 1.1 MHz, 200 kHz < RC/C

; frequency <= 400 kHz.

XOSC0CN\_XFCN\_\_MODE5 EQU 005H ; Select external oscillator mode 5: 1.1 MHz <

; Crystal frequency <= 3.1 MHz, 400 kHz < RC/C

; frequency <= 800 kHz.

XOSC0CN\_XFCN\_\_MODE6 EQU 006H ; Select external oscillator mode 6: 3.1 MHz <

; Crystal frequency <= 8.2 kHz, 800 kHz < RC/C

; frequency <= 1.6 MHz.

XOSC0CN\_XFCN\_\_MODE7 EQU 007H ; Select external oscillator mode 7: 8.2 MHz <

; Crystal frequency <= 25 MHz, 1.6 MHz < RC/C

; frequency <= 3.2 MHz.

XOSC0CN\_XOSCMD\_\_FMASK EQU 070H ; External Oscillator Mode

XOSC0CN\_XOSCMD\_\_SHIFT EQU 004H ; External Oscillator Mode

XOSC0CN\_XOSCMD\_\_DISABLED EQU 000H ; External Oscillator circuit disabled.

XOSC0CN\_XOSCMD\_\_CMOS EQU 020H ; External CMOS Clock Mode.

XOSC0CN\_XOSCMD\_\_CMOS\_DIV\_2 EQU 030H ; External CMOS Clock Mode with divide by 2 stage.

XOSC0CN\_XOSCMD\_\_RC EQU 040H ; RC Oscillator Mode.

XOSC0CN\_XOSCMD\_\_CRYSTAL EQU 060H ; Crystal Oscillator Mode.

XOSC0CN\_XOSCMD\_\_CRYSTAL\_DIV\_2 EQU 070H ; Crystal Oscillator Mode with divide by 2 stage.

XOSC0CN\_XCLKVLD\_\_BMASK EQU 080H ; External Oscillator Valid Flag

XOSC0CN\_XCLKVLD\_\_SHIFT EQU 007H ; External Oscillator Valid Flag

XOSC0CN\_XCLKVLD\_\_NOT\_SET EQU 000H ; External Oscillator is unused or not yet stable.

XOSC0CN\_XCLKVLD\_\_SET EQU 080H ; External Oscillator is running and stable.

;------------------------------------------------------------------------------

; FLKEY Enums (Flash Lock and Key @ 0xB7)

;------------------------------------------------------------------------------

FLKEY\_FLKEY\_\_FMASK EQU 0FFH ; Flash Lock and Key

FLKEY\_FLKEY\_\_SHIFT EQU 000H ; Flash Lock and Key

FLKEY\_FLKEY\_\_LOCKED EQU 000H ; Flash is write/erase locked.

FLKEY\_FLKEY\_\_FIRST EQU 001H ; The first key code has been written (0xA5).

FLKEY\_FLKEY\_\_UNLOCKED EQU 002H ; Flash is unlocked (writes/erases allowed).

FLKEY\_FLKEY\_\_DISABLED EQU 003H ; Flash writes/erases are disabled until the next

; reset.

FLKEY\_FLKEY\_\_KEY1 EQU 0A5H ; Flash writes and erases are enabled by writing

; 0xA5 followed by 0xF1 to the FLKEY register.

FLKEY\_FLKEY\_\_KEY2 EQU 0F1H ; Flash writes and erases are enabled by writing

; 0xA5 followed by 0xF1 to the FLKEY register.

;------------------------------------------------------------------------------

; PSCTL Enums (Program Store Control @ 0x8F)

;------------------------------------------------------------------------------

PSCTL\_PSWE\_\_BMASK EQU 001H ; Program Store Write Enable

PSCTL\_PSWE\_\_SHIFT EQU 000H ; Program Store Write Enable

PSCTL\_PSWE\_\_WRITE\_DISABLED EQU 000H ; Writes to flash program memory disabled.

PSCTL\_PSWE\_\_WRITE\_ENABLED EQU 001H ; Writes to flash program memory enabled; the MOVX

; write instruction targets flash memory.

PSCTL\_PSEE\_\_BMASK EQU 002H ; Program Store Erase Enable

PSCTL\_PSEE\_\_SHIFT EQU 001H ; Program Store Erase Enable

PSCTL\_PSEE\_\_ERASE\_DISABLED EQU 000H ; Flash program memory erasure disabled.

PSCTL\_PSEE\_\_ERASE\_ENABLED EQU 002H ; Flash program memory erasure enabled.

;------------------------------------------------------------------------------

; HFO0CAL Enums (High Frequency Oscillator 0 Calibration @ 0xC7)

;------------------------------------------------------------------------------

HFO0CAL\_HFO0CAL\_\_FMASK EQU 0FFH ; Oscillator Calibration

HFO0CAL\_HFO0CAL\_\_SHIFT EQU 000H ; Oscillator Calibration

;------------------------------------------------------------------------------

; HFO1CAL Enums (High Frequency Oscillator 1 Calibration @ 0xD6)

;------------------------------------------------------------------------------

HFO1CAL\_HFO1CAL\_\_FMASK EQU 07FH ; Oscillator Calibration

HFO1CAL\_HFO1CAL\_\_SHIFT EQU 000H ; Oscillator Calibration

;------------------------------------------------------------------------------

; HFOCN Enums (High Frequency Oscillator Control @ 0xEF)

;------------------------------------------------------------------------------

HFOCN\_HFO0EN\_\_BMASK EQU 008H ; HFOSC0 Oscillator Enable

HFOCN\_HFO0EN\_\_SHIFT EQU 003H ; HFOSC0 Oscillator Enable

HFOCN\_HFO0EN\_\_DISABLED EQU 000H ; Disable High Frequency Oscillator 0 (HFOSC0 will

; still turn on if requested by any block in the

; device or selected as the SYSCLK source).

HFOCN\_HFO0EN\_\_ENABLED EQU 008H ; Force High Frequency Oscillator 0 to run.

HFOCN\_HFO1EN\_\_BMASK EQU 080H ; HFOSC1 Oscillator Enable

HFOCN\_HFO1EN\_\_SHIFT EQU 007H ; HFOSC1 Oscillator Enable

HFOCN\_HFO1EN\_\_DISABLED EQU 000H ; Disable High Frequency Oscillator 1 (HFOSC1 will

; still turn on if requested by any block in the

; device or selected as the SYSCLK source).

HFOCN\_HFO1EN\_\_ENABLED EQU 080H ; Force High Frequency Oscillator 1 to run.

;------------------------------------------------------------------------------

; I2C0ADM Enums (I2C0 Slave Address Mask @ 0xFF)

;------------------------------------------------------------------------------

I2C0ADM\_SLVM\_\_FMASK EQU 07FH ; I2C Hardware Slave Address

I2C0ADM\_SLVM\_\_SHIFT EQU 000H ; I2C Hardware Slave Address

I2C0ADM\_FACS\_\_BMASK EQU 080H ; Force Address Clock Stretching

I2C0ADM\_FACS\_\_SHIFT EQU 007H ; Force Address Clock Stretching

I2C0ADM\_FACS\_\_DONT\_FORCE\_STRETCH EQU 000H ; The I2C0INT bit is not set by acking the slave

; address alone. Additional conditions are required

; to set I2C0INT.

I2C0ADM\_FACS\_\_FORCE\_STRETCH EQU 080H ; The I2C0INT bit is always set when matching slave

; address is acknowledged. This will force clock

; stretching until firmware clears the I2C0INT bit.

;------------------------------------------------------------------------------

; I2C0CN0 Enums (I2C0 Control @ 0xBA)

;------------------------------------------------------------------------------

I2C0CN0\_BUSY\_\_BMASK EQU 001H ; Busy

I2C0CN0\_BUSY\_\_SHIFT EQU 000H ; Busy

I2C0CN0\_BUSY\_\_NOT\_SET EQU 000H ; Device will acknowledge an I2C master.

I2C0CN0\_BUSY\_\_SET EQU 001H ; Device will not respond to an I2C master. All I2C

; data sent to the device will be NACKed.

I2C0CN0\_I2C0EN\_\_BMASK EQU 002H ; I2C Enable

I2C0CN0\_I2C0EN\_\_SHIFT EQU 001H ; I2C Enable

I2C0CN0\_I2C0EN\_\_DISABLED EQU 000H ; Disable the I2C0 Slave module.

I2C0CN0\_I2C0EN\_\_ENABLED EQU 002H ; Enable the I2C0 Slave module.

I2C0CN0\_PRELOAD\_\_BMASK EQU 004H ; Preload Disable

I2C0CN0\_PRELOAD\_\_SHIFT EQU 002H ; Preload Disable

I2C0CN0\_PRELOAD\_\_ENABLED EQU 000H ; Data bytes must be written into the TX FIFO via

; the I2C0DOUT register before the 8th SCL clock of

; the matching slave address byte transfer arrives

; for an I2C read operation.

I2C0CN0\_PRELOAD\_\_DISABLED EQU 004H ; Data bytes need not be preloaded for I2C read

; operations. The data byte can be written to

; I2C0DOUT during interrupt servicing.

I2C0CN0\_TIMEOUT\_\_BMASK EQU 008H ; SCL Low Timeout Enable

I2C0CN0\_TIMEOUT\_\_SHIFT EQU 003H ; SCL Low Timeout Enable

I2C0CN0\_TIMEOUT\_\_DISABLED EQU 000H ; Disable I2C SCL low timeout detection using Timer

; 4.

I2C0CN0\_TIMEOUT\_\_ENABLED EQU 008H ; Enable I2C SCL low timeout detection using Timer 4

; if Timer 4 RLFSEL is set appropriately.

I2C0CN0\_PINMD\_\_BMASK EQU 010H ; Pin Mode Enable

I2C0CN0\_PINMD\_\_SHIFT EQU 004H ; Pin Mode Enable

I2C0CN0\_PINMD\_\_GPIO\_MODE EQU 000H ; Set the I2C0 Slave pins in GPIO mode.

I2C0CN0\_PINMD\_\_I2C\_MODE EQU 010H ; Set the I2C0 Slave pins in I2C mode.

I2C0CN0\_PINDRV\_\_BMASK EQU 020H ; Pin Drive Strength

I2C0CN0\_PINDRV\_\_SHIFT EQU 005H ; Pin Drive Strength

I2C0CN0\_PINDRV\_\_LOW\_DRIVE EQU 000H ; SDA and SCL will use low drive strength.

I2C0CN0\_PINDRV\_\_HIGH\_DRIVE EQU 020H ; SDA and SCL will use high drive strength.

I2C0CN0\_ADDRCHK\_\_BMASK EQU 040H ; Address Check Enable

I2C0CN0\_ADDRCHK\_\_SHIFT EQU 006H ; Address Check Enable

I2C0CN0\_ADDRCHK\_\_DISABLED EQU 000H ; The matching slave address is not copied into the

; receive FIFO.

I2C0CN0\_ADDRCHK\_\_ENABLED EQU 040H ; The matching slave address is copied into the

; receive FIFO.

;------------------------------------------------------------------------------

; I2C0DIN Enums (I2C0 Received Data @ 0xBC)

;------------------------------------------------------------------------------

I2C0DIN\_I2C0DIN\_\_FMASK EQU 0FFH ; I2C0 Received Data

I2C0DIN\_I2C0DIN\_\_SHIFT EQU 000H ; I2C0 Received Data

;------------------------------------------------------------------------------

; I2C0DOUT Enums (I2C0 Transmit Data @ 0xBB)

;------------------------------------------------------------------------------

I2C0DOUT\_I2C0DOUT\_\_FMASK EQU 0FFH ; I2C0 Transmit Data

I2C0DOUT\_I2C0DOUT\_\_SHIFT EQU 000H ; I2C0 Transmit Data

;------------------------------------------------------------------------------

; I2C0FCN0 Enums (I2C0 FIFO Control 0 @ 0xAD)

;------------------------------------------------------------------------------

I2C0FCN0\_RXTH\_\_FMASK EQU 003H ; RX FIFO Threshold

I2C0FCN0\_RXTH\_\_SHIFT EQU 000H ; RX FIFO Threshold

I2C0FCN0\_RXTH\_\_ZERO EQU 000H ; RFRQ will be set anytime new data arrives in the

; RX FIFO (when the RX FIFO is not empty).

I2C0FCN0\_RXTH\_\_ONE EQU 001H ; RFRQ will be set if the RX FIFO contains more than

; one byte.

I2C0FCN0\_RFLSH\_\_BMASK EQU 004H ; RX FIFO Flush

I2C0FCN0\_RFLSH\_\_SHIFT EQU 002H ; RX FIFO Flush

I2C0FCN0\_RFLSH\_\_FLUSH EQU 004H ; Initiate an RX FIFO flush.

I2C0FCN0\_RFRQE\_\_BMASK EQU 008H ; Read Request Interrupt Enable

I2C0FCN0\_RFRQE\_\_SHIFT EQU 003H ; Read Request Interrupt Enable

I2C0FCN0\_RFRQE\_\_DISABLED EQU 000H ; I2C0 interrupts will not be generated when RFRQ is

; set.

I2C0FCN0\_RFRQE\_\_ENABLED EQU 008H ; I2C0 interrupts will be generated if RFRQ is set.

I2C0FCN0\_TXTH\_\_FMASK EQU 030H ; TX FIFO Threshold

I2C0FCN0\_TXTH\_\_SHIFT EQU 004H ; TX FIFO Threshold

I2C0FCN0\_TXTH\_\_ZERO EQU 000H ; TFRQ will be set when the TX FIFO is empty.

I2C0FCN0\_TXTH\_\_ONE EQU 010H ; TFRQ will be set when the TX FIFO contains one or

; fewer bytes.

I2C0FCN0\_TFLSH\_\_BMASK EQU 040H ; TX FIFO Flush

I2C0FCN0\_TFLSH\_\_SHIFT EQU 006H ; TX FIFO Flush

I2C0FCN0\_TFLSH\_\_FLUSH EQU 040H ; Initiate a TX FIFO flush.

I2C0FCN0\_TFRQE\_\_BMASK EQU 080H ; Write Request Interrupt Enable

I2C0FCN0\_TFRQE\_\_SHIFT EQU 007H ; Write Request Interrupt Enable

I2C0FCN0\_TFRQE\_\_DISABLED EQU 000H ; I2C0 interrupts will not be generated when TFRQ is

; set.

I2C0FCN0\_TFRQE\_\_ENABLED EQU 080H ; I2C0 interrupts will be generated if TFRQ is set.

;------------------------------------------------------------------------------

; I2C0FCN1 Enums (I2C0 FIFO Control 1 @ 0xAB)

;------------------------------------------------------------------------------

I2C0FCN1\_RXE\_\_BMASK EQU 004H ; RX FIFO Empty

I2C0FCN1\_RXE\_\_SHIFT EQU 002H ; RX FIFO Empty

I2C0FCN1\_RXE\_\_NOT\_EMPTY EQU 000H ; The RX FIFO contains data.

I2C0FCN1\_RXE\_\_EMPTY EQU 004H ; The RX FIFO is empty.

I2C0FCN1\_RFRQ\_\_BMASK EQU 008H ; Receive FIFO Request

I2C0FCN1\_RFRQ\_\_SHIFT EQU 003H ; Receive FIFO Request

I2C0FCN1\_RFRQ\_\_NOT\_SET EQU 000H ; The number of bytes in the RX FIFO is less than or

; equal to RXTH.

I2C0FCN1\_RFRQ\_\_SET EQU 008H ; The number of bytes in the RX FIFO is greater than

; RXTH.

I2C0FCN1\_TXNF\_\_BMASK EQU 040H ; TX FIFO Not Full

I2C0FCN1\_TXNF\_\_SHIFT EQU 006H ; TX FIFO Not Full

I2C0FCN1\_TXNF\_\_FULL EQU 000H ; The TX FIFO is full.

I2C0FCN1\_TXNF\_\_NOT\_FULL EQU 040H ; The TX FIFO has room for more data.

I2C0FCN1\_TFRQ\_\_BMASK EQU 080H ; Transmit FIFO Request

I2C0FCN1\_TFRQ\_\_SHIFT EQU 007H ; Transmit FIFO Request

I2C0FCN1\_TFRQ\_\_NOT\_SET EQU 000H ; The number of bytes in the TX FIFO is greater than

; TXTH.

I2C0FCN1\_TFRQ\_\_SET EQU 080H ; The number of bytes in the TX FIFO is less than or

; equal to TXTH.

;------------------------------------------------------------------------------

; I2C0FCT Enums (I2C0 FIFO Count @ 0xF5)

;------------------------------------------------------------------------------

I2C0FCT\_RXCNT\_\_FMASK EQU 007H ; RX FIFO Count

I2C0FCT\_RXCNT\_\_SHIFT EQU 000H ; RX FIFO Count

I2C0FCT\_TXCNT\_\_FMASK EQU 070H ; TX FIFO Count

I2C0FCT\_TXCNT\_\_SHIFT EQU 004H ; TX FIFO Count

;------------------------------------------------------------------------------

; I2C0SLAD Enums (I2C0 Slave Address @ 0xBD)

;------------------------------------------------------------------------------

I2C0SLAD\_I2C0SLAD\_\_FMASK EQU 07FH ; I2C Hardware Slave Address

I2C0SLAD\_I2C0SLAD\_\_SHIFT EQU 000H ; I2C Hardware Slave Address

;------------------------------------------------------------------------------

; I2C0STAT Enums (I2C0 Status @ 0xB9)

;------------------------------------------------------------------------------

I2C0STAT\_RD\_\_BMASK EQU 001H ; I2C Read

I2C0STAT\_RD\_\_SHIFT EQU 000H ; I2C Read

I2C0STAT\_RD\_\_NOT\_SET EQU 000H ; An I2C Read operation is not in progress.

I2C0STAT\_RD\_\_SET EQU 001H ; An I2C Read operation is in progress.

I2C0STAT\_WR\_\_BMASK EQU 002H ; I2C Write

I2C0STAT\_WR\_\_SHIFT EQU 001H ; I2C Write

I2C0STAT\_WR\_\_NOT\_SET EQU 000H ; An I2C Write operation is not in progress.

I2C0STAT\_WR\_\_SET EQU 002H ; An I2C Write operation is in progress.

I2C0STAT\_STOP\_\_BMASK EQU 004H ; Stop

I2C0STAT\_STOP\_\_SHIFT EQU 002H ; Stop

I2C0STAT\_STOP\_\_NOT\_SET EQU 000H ; A STOP is not pending.

I2C0STAT\_STOP\_\_SET EQU 004H ; A STOP is currently pending for the I2C0 Slave.

I2C0STAT\_START\_\_BMASK EQU 008H ; Start

I2C0STAT\_START\_\_SHIFT EQU 003H ; Start

I2C0STAT\_START\_\_NOT\_SET EQU 000H ; A START was not detected.

I2C0STAT\_START\_\_SET EQU 008H ; A START is currently pending for the I2C0 Slave.

I2C0STAT\_NACK\_\_BMASK EQU 010H ; NACK

I2C0STAT\_NACK\_\_SHIFT EQU 004H ; NACK

I2C0STAT\_NACK\_\_NOT\_SET EQU 000H ; A NACK did not occur.

I2C0STAT\_NACK\_\_SET EQU 010H ; A NACK occurred.

I2C0STAT\_I2C0INT\_\_BMASK EQU 020H ; I2C Interrupt

I2C0STAT\_I2C0INT\_\_SHIFT EQU 005H ; I2C Interrupt

I2C0STAT\_I2C0INT\_\_NOT\_SET EQU 000H ; An interrupt did not occur.

I2C0STAT\_I2C0INT\_\_SET EQU 020H ; An interrupt occurred.

I2C0STAT\_ACTIVE\_\_BMASK EQU 040H ; Bus Active

I2C0STAT\_ACTIVE\_\_SHIFT EQU 006H ; Bus Active

I2C0STAT\_ACTIVE\_\_NOT\_SET EQU 000H ; A transfer is not in progress.

I2C0STAT\_ACTIVE\_\_SET EQU 040H ; A transfer is in progress.

I2C0STAT\_HSMODE\_\_BMASK EQU 080H ; High Speed Mode

I2C0STAT\_HSMODE\_\_SHIFT EQU 007H ; High Speed Mode

I2C0STAT\_HSMODE\_\_NOT\_SET EQU 000H ; A High Speed transfer is not in progress.

I2C0STAT\_HSMODE\_\_SET EQU 080H ; A High Speed transfer is in progress.

;------------------------------------------------------------------------------

; EIE1 Enums (Extended Interrupt Enable 1 @ 0xE6)

;------------------------------------------------------------------------------

EIE1\_ESMB0\_\_BMASK EQU 001H ; SMBus (SMB0) Interrupt Enable

EIE1\_ESMB0\_\_SHIFT EQU 000H ; SMBus (SMB0) Interrupt Enable

EIE1\_ESMB0\_\_DISABLED EQU 000H ; Disable all SMB0 interrupts.

EIE1\_ESMB0\_\_ENABLED EQU 001H ; Enable interrupt requests generated by SMB0.

EIE1\_EMAT\_\_BMASK EQU 002H ; Port Match Interrupts Enable

EIE1\_EMAT\_\_SHIFT EQU 001H ; Port Match Interrupts Enable

EIE1\_EMAT\_\_DISABLED EQU 000H ; Disable all Port Match interrupts.

EIE1\_EMAT\_\_ENABLED EQU 002H ; Enable interrupt requests generated by a Port

; Match.

EIE1\_EWADC0\_\_BMASK EQU 004H ; ADC0 Window Comparison Interrupt Enable

EIE1\_EWADC0\_\_SHIFT EQU 002H ; ADC0 Window Comparison Interrupt Enable

EIE1\_EWADC0\_\_DISABLED EQU 000H ; Disable ADC0 Window Comparison interrupt.

EIE1\_EWADC0\_\_ENABLED EQU 004H ; Enable interrupt requests generated by ADC0 Window

; Compare flag (ADWINT).

EIE1\_EADC0\_\_BMASK EQU 008H ; ADC0 Conversion Complete Interrupt Enable

EIE1\_EADC0\_\_SHIFT EQU 003H ; ADC0 Conversion Complete Interrupt Enable

EIE1\_EADC0\_\_DISABLED EQU 000H ; Disable ADC0 Conversion Complete interrupt.

EIE1\_EADC0\_\_ENABLED EQU 008H ; Enable interrupt requests generated by the ADINT

; flag.

EIE1\_EPCA0\_\_BMASK EQU 010H ; Programmable Counter Array (PCA0) Interrupt Enable

EIE1\_EPCA0\_\_SHIFT EQU 004H ; Programmable Counter Array (PCA0) Interrupt Enable

EIE1\_EPCA0\_\_DISABLED EQU 000H ; Disable all PCA0 interrupts.

EIE1\_EPCA0\_\_ENABLED EQU 010H ; Enable interrupt requests generated by PCA0.

EIE1\_ECP0\_\_BMASK EQU 020H ; Comparator0 (CP0) Interrupt Enable

EIE1\_ECP0\_\_SHIFT EQU 005H ; Comparator0 (CP0) Interrupt Enable

EIE1\_ECP0\_\_DISABLED EQU 000H ; Disable CP0 interrupts.

EIE1\_ECP0\_\_ENABLED EQU 020H ; Enable interrupt requests generated by the

; comparator 0 CPRIF or CPFIF flags.

EIE1\_ECP1\_\_BMASK EQU 040H ; Comparator1 (CP1) Interrupt Enable

EIE1\_ECP1\_\_SHIFT EQU 006H ; Comparator1 (CP1) Interrupt Enable

EIE1\_ECP1\_\_DISABLED EQU 000H ; Disable CP1 interrupts.

EIE1\_ECP1\_\_ENABLED EQU 040H ; Enable interrupt requests generated by the

; comparator 1 CPRIF or CPFIF flags.

EIE1\_ET3\_\_BMASK EQU 080H ; Timer 3 Interrupt Enable

EIE1\_ET3\_\_SHIFT EQU 007H ; Timer 3 Interrupt Enable

EIE1\_ET3\_\_DISABLED EQU 000H ; Disable Timer 3 interrupts.

EIE1\_ET3\_\_ENABLED EQU 080H ; Enable interrupt requests generated by the TF3L or

; TF3H flags.

;------------------------------------------------------------------------------

; EIE2 Enums (Extended Interrupt Enable 2 @ 0xF3)

;------------------------------------------------------------------------------

EIE2\_ES1\_\_BMASK EQU 001H ; UART1 Interrupt Enable

EIE2\_ES1\_\_SHIFT EQU 000H ; UART1 Interrupt Enable

EIE2\_ES1\_\_DISABLED EQU 000H ; Disable UART1 interrupts.

EIE2\_ES1\_\_ENABLED EQU 001H ; Enable UART1 interrupts.

EIE2\_EI2C0\_\_BMASK EQU 002H ; I2C0 Slave Interrupt Enable

EIE2\_EI2C0\_\_SHIFT EQU 001H ; I2C0 Slave Interrupt Enable

EIE2\_EI2C0\_\_DISABLED EQU 000H ; Disable all I2C0 slave interrupts.

EIE2\_EI2C0\_\_ENABLED EQU 002H ; Enable interrupt requests generated by the I2C0

; slave.

EIE2\_ET4\_\_BMASK EQU 004H ; Timer 4 Interrupt Enable

EIE2\_ET4\_\_SHIFT EQU 002H ; Timer 4 Interrupt Enable

EIE2\_ET4\_\_DISABLED EQU 000H ; Disable Timer 4 interrupts.

EIE2\_ET4\_\_ENABLED EQU 004H ; Enable interrupt requests generated by the TF4L or

; TF4H flags.

EIE2\_ET5\_\_BMASK EQU 008H ; Timer 5 Interrupt Enable

EIE2\_ET5\_\_SHIFT EQU 003H ; Timer 5 Interrupt Enable

EIE2\_ET5\_\_DISABLED EQU 000H ; Disable Timer 5 interrupts.

EIE2\_ET5\_\_ENABLED EQU 008H ; Enable interrupt requests generated by the TF5L or

; TF5H flags.

EIE2\_CL0\_\_BMASK EQU 010H ; Configurable Logic (CL0) Interrupt Enable

EIE2\_CL0\_\_SHIFT EQU 004H ; Configurable Logic (CL0) Interrupt Enable

EIE2\_CL0\_\_DISABLED EQU 000H ; Disable CL0 interrupts.

EIE2\_CL0\_\_ENABLED EQU 010H ; Enable interrupt requests generated by CL0.

;------------------------------------------------------------------------------

; EIP1 Enums (Extended Interrupt Priority 1 Low @ 0xBB)

;------------------------------------------------------------------------------

EIP1\_PSMB0\_\_BMASK EQU 001H ; SMBus (SMB0) Interrupt Priority Control LSB

EIP1\_PSMB0\_\_SHIFT EQU 000H ; SMBus (SMB0) Interrupt Priority Control LSB

EIP1\_PSMB0\_\_LOW EQU 000H ; SMB0 interrupt priority LSB set to low.

EIP1\_PSMB0\_\_HIGH EQU 001H ; SMB0 interrupt priority LSB set to high.

EIP1\_PMAT\_\_BMASK EQU 002H ; Port Match Interrupt Priority Control LSB

EIP1\_PMAT\_\_SHIFT EQU 001H ; Port Match Interrupt Priority Control LSB

EIP1\_PMAT\_\_LOW EQU 000H ; Port Match interrupt priority LSB set to low.

EIP1\_PMAT\_\_HIGH EQU 002H ; Port Match interrupt priority LSB set to high.

EIP1\_PWADC0\_\_BMASK EQU 004H ; ADC0 Window Comparator Interrupt Priority Control LSB

EIP1\_PWADC0\_\_SHIFT EQU 002H ; ADC0 Window Comparator Interrupt Priority Control LSB

EIP1\_PWADC0\_\_LOW EQU 000H ; ADC0 Window interrupt priority LSB set to low.

EIP1\_PWADC0\_\_HIGH EQU 004H ; ADC0 Window interrupt priority LSB set to high.

EIP1\_PADC0\_\_BMASK EQU 008H ; ADC0 Conversion Complete Interrupt Priority Control LSB

EIP1\_PADC0\_\_SHIFT EQU 003H ; ADC0 Conversion Complete Interrupt Priority Control LSB

EIP1\_PADC0\_\_LOW EQU 000H ; ADC0 Conversion Complete interrupt priority LSB

; set to low.

EIP1\_PADC0\_\_HIGH EQU 008H ; ADC0 Conversion Complete interrupt priority LSB

; set to high.

EIP1\_PPCA0\_\_BMASK EQU 010H ; Programmable Counter Array (PCA0) Interrupt Priority Control LSB

EIP1\_PPCA0\_\_SHIFT EQU 004H ; Programmable Counter Array (PCA0) Interrupt Priority Control LSB

EIP1\_PPCA0\_\_LOW EQU 000H ; PCA0 interrupt priority LSB set to low.

EIP1\_PPCA0\_\_HIGH EQU 010H ; PCA0 interrupt priority LSB set to high.

EIP1\_PCP0\_\_BMASK EQU 020H ; Comparator0 (CP0) Interrupt Priority Control LSB

EIP1\_PCP0\_\_SHIFT EQU 005H ; Comparator0 (CP0) Interrupt Priority Control LSB

EIP1\_PCP0\_\_LOW EQU 000H ; CP0 interrupt priority LSB set to low.

EIP1\_PCP0\_\_HIGH EQU 020H ; CP0 interrupt priority LSB set to high.

EIP1\_PCP1\_\_BMASK EQU 040H ; Comparator1 (CP1) Interrupt Priority Control LSB

EIP1\_PCP1\_\_SHIFT EQU 006H ; Comparator1 (CP1) Interrupt Priority Control LSB

EIP1\_PCP1\_\_LOW EQU 000H ; CP1 interrupt priority LSB set to low.

EIP1\_PCP1\_\_HIGH EQU 040H ; CP1 interrupt priority LSB set to high.

EIP1\_PT3\_\_BMASK EQU 080H ; Timer 3 Interrupt Priority Control LSB

EIP1\_PT3\_\_SHIFT EQU 007H ; Timer 3 Interrupt Priority Control LSB

EIP1\_PT3\_\_LOW EQU 000H ; Timer 3 interrupt priority LSB set to low.

EIP1\_PT3\_\_HIGH EQU 080H ; Timer 3 interrupt priority LSB set to high.

;------------------------------------------------------------------------------

; EIP1H Enums (Extended Interrupt Priority 1 High @ 0xEE)

;------------------------------------------------------------------------------

EIP1H\_PHSMB0\_\_BMASK EQU 001H ; SMBus (SMB0) Interrupt Priority Control MSB

EIP1H\_PHSMB0\_\_SHIFT EQU 000H ; SMBus (SMB0) Interrupt Priority Control MSB

EIP1H\_PHSMB0\_\_LOW EQU 000H ; SMB0 interrupt priority MSB set to low.

EIP1H\_PHSMB0\_\_HIGH EQU 001H ; SMB0 interrupt priority MSB set to high.

EIP1H\_PHMAT\_\_BMASK EQU 002H ; Port Match Interrupt Priority Control MSB

EIP1H\_PHMAT\_\_SHIFT EQU 001H ; Port Match Interrupt Priority Control MSB

EIP1H\_PHMAT\_\_LOW EQU 000H ; Port Match interrupt priority MSB set to low.

EIP1H\_PHMAT\_\_HIGH EQU 002H ; Port Match interrupt priority MSB set to high.

EIP1H\_PHWADC0\_\_BMASK EQU 004H ; ADC0 Window Comparator Interrupt Priority Control MSB

EIP1H\_PHWADC0\_\_SHIFT EQU 002H ; ADC0 Window Comparator Interrupt Priority Control MSB

EIP1H\_PHWADC0\_\_LOW EQU 000H ; ADC0 Window interrupt priority MSB set to low.

EIP1H\_PHWADC0\_\_HIGH EQU 004H ; ADC0 Window interrupt priority MSB set to high.

EIP1H\_PHADC0\_\_BMASK EQU 008H ; ADC0 Conversion Complete Interrupt Priority Control MSB

EIP1H\_PHADC0\_\_SHIFT EQU 003H ; ADC0 Conversion Complete Interrupt Priority Control MSB

EIP1H\_PHADC0\_\_LOW EQU 000H ; ADC0 Conversion Complete interrupt priority MSB

; set to low.

EIP1H\_PHADC0\_\_HIGH EQU 008H ; ADC0 Conversion Complete interrupt priority MSB

; set to high.

EIP1H\_PHPCA0\_\_BMASK EQU 010H ; Programmable Counter Array (PCA0) Interrupt Priority Control MSB

EIP1H\_PHPCA0\_\_SHIFT EQU 004H ; Programmable Counter Array (PCA0) Interrupt Priority Control MSB

EIP1H\_PHPCA0\_\_LOW EQU 000H ; PCA0 interrupt priority MSB set to low.

EIP1H\_PHPCA0\_\_HIGH EQU 010H ; PCA0 interrupt priority MSB set to high.

EIP1H\_PHCP0\_\_BMASK EQU 020H ; Comparator0 (CP0) Interrupt Priority Control MSB

EIP1H\_PHCP0\_\_SHIFT EQU 005H ; Comparator0 (CP0) Interrupt Priority Control MSB

EIP1H\_PHCP0\_\_LOW EQU 000H ; CP0 interrupt priority MSB set to low.

EIP1H\_PHCP0\_\_HIGH EQU 020H ; CP0 interrupt priority MSB set to high.

EIP1H\_PHCP1\_\_BMASK EQU 040H ; Comparator1 (CP1) Interrupt Priority Control MSB

EIP1H\_PHCP1\_\_SHIFT EQU 006H ; Comparator1 (CP1) Interrupt Priority Control MSB

EIP1H\_PHCP1\_\_LOW EQU 000H ; CP1 interrupt priority MSB set to low.

EIP1H\_PHCP1\_\_HIGH EQU 040H ; CP1 interrupt priority MSB set to high.

EIP1H\_PHT3\_\_BMASK EQU 080H ; Timer 3 Interrupt Priority Control MSB

EIP1H\_PHT3\_\_SHIFT EQU 007H ; Timer 3 Interrupt Priority Control MSB

EIP1H\_PHT3\_\_LOW EQU 000H ; Timer 3 interrupt priority MSB set to low.

EIP1H\_PHT3\_\_HIGH EQU 080H ; Timer 3 interrupt priority MSB set to high.

;------------------------------------------------------------------------------

; EIP2 Enums (Extended Interrupt Priority 2 @ 0xED)

;------------------------------------------------------------------------------

EIP2\_PS1\_\_BMASK EQU 001H ; UART1 Interrupt Priority Control LSB

EIP2\_PS1\_\_SHIFT EQU 000H ; UART1 Interrupt Priority Control LSB

EIP2\_PS1\_\_LOW EQU 000H ; UART1 interrupt priority LSB set to low.

EIP2\_PS1\_\_HIGH EQU 001H ; UART1 interrupt priority LSB set to high.

EIP2\_PI2C0\_\_BMASK EQU 002H ; I2C0 Slave Interrupt Priority Control LSB

EIP2\_PI2C0\_\_SHIFT EQU 001H ; I2C0 Slave Interrupt Priority Control LSB

EIP2\_PI2C0\_\_LOW EQU 000H ; I2C0 Slave interrupt priority LSB set to low.

EIP2\_PI2C0\_\_HIGH EQU 002H ; I2C0 Slave interrupt priority LSB set to high.

EIP2\_PT4\_\_BMASK EQU 004H ; Timer 4 Interrupt Priority Control LSB

EIP2\_PT4\_\_SHIFT EQU 002H ; Timer 4 Interrupt Priority Control LSB

EIP2\_PT4\_\_LOW EQU 000H ; Timer 4 interrupt priority LSB set to low.

EIP2\_PT4\_\_HIGH EQU 004H ; Timer 4 interrupt priority LSB set to high.

EIP2\_PT5\_\_BMASK EQU 008H ; Timer 5 Interrupt Priority Control LSB

EIP2\_PT5\_\_SHIFT EQU 003H ; Timer 5 Interrupt Priority Control LSB

EIP2\_PT5\_\_LOW EQU 000H ; Timer 5 interrupt priority LSB set to low.

EIP2\_PT5\_\_HIGH EQU 008H ; Timer 5 interrupt priority LSB set to high.

EIP2\_PCL0\_\_BMASK EQU 010H ; Configurable Logic (CL0) Interrupt Priority Control LSB

EIP2\_PCL0\_\_SHIFT EQU 004H ; Configurable Logic (CL0) Interrupt Priority Control LSB

EIP2\_PCL0\_\_LOW EQU 000H ; CL0 interrupt priority LSB set to low.

EIP2\_PCL0\_\_HIGH EQU 010H ; CL0 interrupt priority LSB set to high.

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; EIP2H Enums (Extended Interrupt Priority 2 High @ 0xF6)

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EIP2H\_PHS1\_\_BMASK EQU 001H ; UART1 Interrupt Priority Control MSB

EIP2H\_PHS1\_\_SHIFT EQU 000H ; UART1 Interrupt Priority Control MSB

EIP2H\_PHS1\_\_LOW EQU 000H ; UART1 interrupt priority MSB set to low.

EIP2H\_PHS1\_\_HIGH EQU 001H ; UART1 interrupt priority MSB set to high.

EIP2H\_PHI2C0\_\_BMASK EQU 002H ; I2C0 Slave Interrupt Priority Control MSB

EIP2H\_PHI2C0\_\_SHIFT EQU 001H ; I2C0 Slave Interrupt Priority Control MSB

EIP2H\_PHI2C0\_\_LOW EQU 000H ; I2C0 Slave interrupt priority MSB set to low.

EIP2H\_PHI2C0\_\_HIGH EQU 002H ; I2C0 Slave interrupt priority MSB set to high.

EIP2H\_PHT4\_\_BMASK EQU 004H ; Timer 4 Interrupt Priority Control MSB

EIP2H\_PHT4\_\_SHIFT EQU 002H ; Timer 4 Interrupt Priority Control MSB

EIP2H\_PHT4\_\_LOW EQU 000H ; Timer 4 interrupt priority MSB set to low.

EIP2H\_PHT4\_\_HIGH EQU 004H ; Timer 4 interrupt priority MSB set to high.

EIP2H\_PHT5\_\_BMASK EQU 008H ; Timer 5 Interrupt Priority Control MSB

EIP2H\_PHT5\_\_SHIFT EQU 003H ; Timer 5 Interrupt Priority Control MSB

EIP2H\_PHT5\_\_LOW EQU 000H ; Timer 5 interrupt priority MSB set to low.

EIP2H\_PHT5\_\_HIGH EQU 008H ; Timer 5 interrupt priority MSB set to high.

EIP2H\_PHCL0\_\_BMASK EQU 010H ; Configurable Logic (CL0) Interrupt Priority Control MSB

EIP2H\_PHCL0\_\_SHIFT EQU 004H ; Configurable Logic (CL0) Interrupt Priority Control MSB

EIP2H\_PHCL0\_\_LOW EQU 000H ; CL0 interrupt priority MSB set to low.

EIP2H\_PHCL0\_\_HIGH EQU 010H ; CL0 interrupt priority MSB set to high.

;------------------------------------------------------------------------------

; IE Enums (Interrupt Enable @ 0xA8)

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IE\_EX0\_\_BMASK EQU 001H ; External Interrupt 0 Enable

IE\_EX0\_\_SHIFT EQU 000H ; External Interrupt 0 Enable

IE\_EX0\_\_DISABLED EQU 000H ; Disable external interrupt 0.

IE\_EX0\_\_ENABLED EQU 001H ; Enable interrupt requests generated by the INT0

; input.

IE\_ET0\_\_BMASK EQU 002H ; Timer 0 Interrupt Enable

IE\_ET0\_\_SHIFT EQU 001H ; Timer 0 Interrupt Enable

IE\_ET0\_\_DISABLED EQU 000H ; Disable all Timer 0 interrupt.

IE\_ET0\_\_ENABLED EQU 002H ; Enable interrupt requests generated by the TF0

; flag.

IE\_EX1\_\_BMASK EQU 004H ; External Interrupt 1 Enable

IE\_EX1\_\_SHIFT EQU 002H ; External Interrupt 1 Enable

IE\_EX1\_\_DISABLED EQU 000H ; Disable external interrupt 1.

IE\_EX1\_\_ENABLED EQU 004H ; Enable interrupt requests generated by the INT1

; input.

IE\_ET1\_\_BMASK EQU 008H ; Timer 1 Interrupt Enable

IE\_ET1\_\_SHIFT EQU 003H ; Timer 1 Interrupt Enable

IE\_ET1\_\_DISABLED EQU 000H ; Disable all Timer 1 interrupt.

IE\_ET1\_\_ENABLED EQU 008H ; Enable interrupt requests generated by the TF1

; flag.

IE\_ES0\_\_BMASK EQU 010H ; UART0 Interrupt Enable

IE\_ES0\_\_SHIFT EQU 004H ; UART0 Interrupt Enable

IE\_ES0\_\_DISABLED EQU 000H ; Disable UART0 interrupt.

IE\_ES0\_\_ENABLED EQU 010H ; Enable UART0 interrupt.

IE\_ET2\_\_BMASK EQU 020H ; Timer 2 Interrupt Enable

IE\_ET2\_\_SHIFT EQU 005H ; Timer 2 Interrupt Enable

IE\_ET2\_\_DISABLED EQU 000H ; Disable Timer 2 interrupt.

IE\_ET2\_\_ENABLED EQU 020H ; Enable interrupt requests generated by the TF2L or

; TF2H flags.

IE\_ESPI0\_\_BMASK EQU 040H ; SPI0 Interrupt Enable

IE\_ESPI0\_\_SHIFT EQU 006H ; SPI0 Interrupt Enable

IE\_ESPI0\_\_DISABLED EQU 000H ; Disable all SPI0 interrupts.

IE\_ESPI0\_\_ENABLED EQU 040H ; Enable interrupt requests generated by SPI0.

IE\_EA\_\_BMASK EQU 080H ; All Interrupts Enable

IE\_EA\_\_SHIFT EQU 007H ; All Interrupts Enable

IE\_EA\_\_DISABLED EQU 000H ; Disable all interrupt sources.

IE\_EA\_\_ENABLED EQU 080H ; Enable each interrupt according to its individual

; mask setting.

;------------------------------------------------------------------------------

; IP Enums (Interrupt Priority @ 0xB8)

;------------------------------------------------------------------------------

IP\_PX0\_\_BMASK EQU 001H ; External Interrupt 0 Priority Control LSB

IP\_PX0\_\_SHIFT EQU 000H ; External Interrupt 0 Priority Control LSB

IP\_PX0\_\_LOW EQU 000H ; External Interrupt 0 priority LSB set to low.

IP\_PX0\_\_HIGH EQU 001H ; External Interrupt 0 priority LSB set to high.

IP\_PT0\_\_BMASK EQU 002H ; Timer 0 Interrupt Priority Control LSB

IP\_PT0\_\_SHIFT EQU 001H ; Timer 0 Interrupt Priority Control LSB

IP\_PT0\_\_LOW EQU 000H ; Timer 0 interrupt priority LSB set to low.

IP\_PT0\_\_HIGH EQU 002H ; Timer 0 interrupt priority LSB set to high.

IP\_PX1\_\_BMASK EQU 004H ; External Interrupt 1 Priority Control LSB

IP\_PX1\_\_SHIFT EQU 002H ; External Interrupt 1 Priority Control LSB

IP\_PX1\_\_LOW EQU 000H ; External Interrupt 1 priority LSB set to low.

IP\_PX1\_\_HIGH EQU 004H ; External Interrupt 1 priority LSB set to high.

IP\_PT1\_\_BMASK EQU 008H ; Timer 1 Interrupt Priority Control LSB

IP\_PT1\_\_SHIFT EQU 003H ; Timer 1 Interrupt Priority Control LSB

IP\_PT1\_\_LOW EQU 000H ; Timer 1 interrupt priority LSB set to low.

IP\_PT1\_\_HIGH EQU 008H ; Timer 1 interrupt priority LSB set to high.

IP\_PS0\_\_BMASK EQU 010H ; UART0 Interrupt Priority Control LSB

IP\_PS0\_\_SHIFT EQU 004H ; UART0 Interrupt Priority Control LSB

IP\_PS0\_\_LOW EQU 000H ; UART0 interrupt priority LSB set to low.

IP\_PS0\_\_HIGH EQU 010H ; UART0 interrupt priority LSB set to high.

IP\_PT2\_\_BMASK EQU 020H ; Timer 2 Interrupt Priority Control LSB

IP\_PT2\_\_SHIFT EQU 005H ; Timer 2 Interrupt Priority Control LSB

IP\_PT2\_\_LOW EQU 000H ; Timer 2 interrupt priority LSB set to low.

IP\_PT2\_\_HIGH EQU 020H ; Timer 2 interrupt priority LSB set to high.

IP\_PSPI0\_\_BMASK EQU 040H ; Serial Peripheral Interface (SPI0) Interrupt Priority Control LSB

IP\_PSPI0\_\_SHIFT EQU 006H ; Serial Peripheral Interface (SPI0) Interrupt Priority Control LSB

IP\_PSPI0\_\_LOW EQU 000H ; SPI0 interrupt priority LSB set to low.

IP\_PSPI0\_\_HIGH EQU 040H ; SPI0 interrupt priority LSB set to high.

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; IPH Enums (Interrupt Priority High @ 0xF2)

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IPH\_PHX0\_\_BMASK EQU 001H ; External Interrupt 0 Priority Control MSB

IPH\_PHX0\_\_SHIFT EQU 000H ; External Interrupt 0 Priority Control MSB

IPH\_PHX0\_\_LOW EQU 000H ; External Interrupt 0 priority MSB set to low.

IPH\_PHX0\_\_HIGH EQU 001H ; External Interrupt 0 priority MSB set to high.

IPH\_PHT0\_\_BMASK EQU 002H ; Timer 0 Interrupt Priority Control MSB

IPH\_PHT0\_\_SHIFT EQU 001H ; Timer 0 Interrupt Priority Control MSB

IPH\_PHT0\_\_LOW EQU 000H ; Timer 0 interrupt priority MSB set to low.

IPH\_PHT0\_\_HIGH EQU 002H ; Timer 0 interrupt priority MSB set to high.

IPH\_PHX1\_\_BMASK EQU 004H ; External Interrupt 1 Priority Control MSB

IPH\_PHX1\_\_SHIFT EQU 002H ; External Interrupt 1 Priority Control MSB

IPH\_PHX1\_\_LOW EQU 000H ; External Interrupt 1 priority MSB set to low.

IPH\_PHX1\_\_HIGH EQU 004H ; External Interrupt 1 priority MSB set to high.

IPH\_PHT1\_\_BMASK EQU 008H ; Timer 1 Interrupt Priority Control MSB

IPH\_PHT1\_\_SHIFT EQU 003H ; Timer 1 Interrupt Priority Control MSB

IPH\_PHT1\_\_LOW EQU 000H ; Timer 1 interrupt priority MSB set to low.

IPH\_PHT1\_\_HIGH EQU 008H ; Timer 1 interrupt priority MSB set to high.

IPH\_PHS0\_\_BMASK EQU 010H ; UART0 Interrupt Priority Control MSB

IPH\_PHS0\_\_SHIFT EQU 004H ; UART0 Interrupt Priority Control MSB

IPH\_PHS0\_\_LOW EQU 000H ; UART0 interrupt priority MSB set to low.

IPH\_PHS0\_\_HIGH EQU 010H ; UART0 interrupt priority MSB set to high.

IPH\_PHT2\_\_BMASK EQU 020H ; Timer 2 Interrupt Priority Control MSB

IPH\_PHT2\_\_SHIFT EQU 005H ; Timer 2 Interrupt Priority Control MSB

IPH\_PHT2\_\_LOW EQU 000H ; Timer 2 interrupt priority MSB set to low.

IPH\_PHT2\_\_HIGH EQU 020H ; Timer 2 interrupt priority MSB set to high.

IPH\_PHSPI0\_\_BMASK EQU 040H ; Serial Peripheral Interface (SPI0) Interrupt Priority Control MSB

IPH\_PHSPI0\_\_SHIFT EQU 006H ; Serial Peripheral Interface (SPI0) Interrupt Priority Control MSB

IPH\_PHSPI0\_\_LOW EQU 000H ; SPI0 interrupt priority MSB set to low.

IPH\_PHSPI0\_\_HIGH EQU 040H ; SPI0 interrupt priority MSB set to high.

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; LFO0CN Enums (Low Frequency Oscillator Control @ 0xB1)

;------------------------------------------------------------------------------

LFO0CN\_OSCLD\_\_FMASK EQU 003H ; Internal L-F Oscillator Divider Select

LFO0CN\_OSCLD\_\_SHIFT EQU 000H ; Internal L-F Oscillator Divider Select

LFO0CN\_OSCLD\_\_DIVIDE\_BY\_8 EQU 000H ; Divide by 8 selected.

LFO0CN\_OSCLD\_\_DIVIDE\_BY\_4 EQU 001H ; Divide by 4 selected.

LFO0CN\_OSCLD\_\_DIVIDE\_BY\_2 EQU 002H ; Divide by 2 selected.

LFO0CN\_OSCLD\_\_DIVIDE\_BY\_1 EQU 003H ; Divide by 1 selected.

LFO0CN\_OSCLF\_\_FMASK EQU 03CH ; Internal L-F Oscillator Frequency Control

LFO0CN\_OSCLF\_\_SHIFT EQU 002H ; Internal L-F Oscillator Frequency Control

LFO0CN\_OSCLRDY\_\_BMASK EQU 040H ; Internal L-F Oscillator Ready

LFO0CN\_OSCLRDY\_\_SHIFT EQU 006H ; Internal L-F Oscillator Ready

LFO0CN\_OSCLRDY\_\_NOT\_SET EQU 000H ; Internal L-F Oscillator frequency not stabilized.

LFO0CN\_OSCLRDY\_\_SET EQU 040H ; Internal L-F Oscillator frequency stabilized.

LFO0CN\_OSCLEN\_\_BMASK EQU 080H ; Internal L-F Oscillator Enable

LFO0CN\_OSCLEN\_\_SHIFT EQU 007H ; Internal L-F Oscillator Enable

LFO0CN\_OSCLEN\_\_DISABLED EQU 000H ; Internal L-F Oscillator Disabled.

LFO0CN\_OSCLEN\_\_ENABLED EQU 080H ; Internal L-F Oscillator Enabled.

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; PRTDRV Enums (Port Drive Strength @ 0xF6)

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PRTDRV\_P0DRV\_\_BMASK EQU 001H ; Port 0 Drive Strength

PRTDRV\_P0DRV\_\_SHIFT EQU 000H ; Port 0 Drive Strength

PRTDRV\_P0DRV\_\_LOW\_DRIVE EQU 000H ; All pins on P0 use low drive strength.

PRTDRV\_P0DRV\_\_HIGH\_DRIVE EQU 001H ; All pins on P0 use high drive strength.

PRTDRV\_P1DRV\_\_BMASK EQU 002H ; Port 1 Drive Strength

PRTDRV\_P1DRV\_\_SHIFT EQU 001H ; Port 1 Drive Strength

PRTDRV\_P1DRV\_\_LOW\_DRIVE EQU 000H ; All pins on P1 use low drive strength.

PRTDRV\_P1DRV\_\_HIGH\_DRIVE EQU 002H ; All pins on P1 use high drive strength.

PRTDRV\_P2DRV\_\_BMASK EQU 004H ; Port 2 Drive Strength

PRTDRV\_P2DRV\_\_SHIFT EQU 002H ; Port 2 Drive Strength

PRTDRV\_P2DRV\_\_LOW\_DRIVE EQU 000H ; All pins on P2 use low drive strength.

PRTDRV\_P2DRV\_\_HIGH\_DRIVE EQU 004H ; All pins on P2 use high drive strength.

PRTDRV\_P3DRV\_\_BMASK EQU 008H ; Port 3 Drive Strength

PRTDRV\_P3DRV\_\_SHIFT EQU 003H ; Port 3 Drive Strength

PRTDRV\_P3DRV\_\_LOW\_DRIVE EQU 000H ; All pins on P3 use low drive strength.

PRTDRV\_P3DRV\_\_HIGH\_DRIVE EQU 008H ; All pins on P3 use high drive strength.

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; XBR0 Enums (Port I/O Crossbar 0 @ 0xE1)

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XBR0\_URT0E\_\_BMASK EQU 001H ; UART0 I/O Enable

XBR0\_URT0E\_\_SHIFT EQU 000H ; UART0 I/O Enable

XBR0\_URT0E\_\_DISABLED EQU 000H ; UART0 I/O unavailable at Port pin.

XBR0\_URT0E\_\_ENABLED EQU 001H ; UART0 TX0, RX0 routed to Port pins P0.4 and P0.5.

XBR0\_SPI0E\_\_BMASK EQU 002H ; SPI I/O Enable

XBR0\_SPI0E\_\_SHIFT EQU 001H ; SPI I/O Enable

XBR0\_SPI0E\_\_DISABLED EQU 000H ; SPI I/O unavailable at Port pins.

XBR0\_SPI0E\_\_ENABLED EQU 002H ; SPI I/O routed to Port pins. The SPI can be

; assigned either 3 or 4 GPIO pins.

XBR0\_SMB0E\_\_BMASK EQU 004H ; SMB0 I/O Enable

XBR0\_SMB0E\_\_SHIFT EQU 002H ; SMB0 I/O Enable

XBR0\_SMB0E\_\_DISABLED EQU 000H ; SMBus 0 I/O unavailable at Port pins.

XBR0\_SMB0E\_\_ENABLED EQU 004H ; SMBus 0 I/O routed to Port pins.

XBR0\_CP0E\_\_BMASK EQU 008H ; Comparator0 Output Enable

XBR0\_CP0E\_\_SHIFT EQU 003H ; Comparator0 Output Enable

XBR0\_CP0E\_\_DISABLED EQU 000H ; CP0 unavailable at Port pin.

XBR0\_CP0E\_\_ENABLED EQU 008H ; CP0 routed to Port pin.

XBR0\_CP0AE\_\_BMASK EQU 010H ; Comparator0 Asynchronous Output Enable

XBR0\_CP0AE\_\_SHIFT EQU 004H ; Comparator0 Asynchronous Output Enable

XBR0\_CP0AE\_\_DISABLED EQU 000H ; Asynchronous CP0 unavailable at Port pin.

XBR0\_CP0AE\_\_ENABLED EQU 010H ; Asynchronous CP0 routed to Port pin.

XBR0\_CP1E\_\_BMASK EQU 020H ; Comparator1 Output Enable

XBR0\_CP1E\_\_SHIFT EQU 005H ; Comparator1 Output Enable

XBR0\_CP1E\_\_DISABLED EQU 000H ; CP1 unavailable at Port pin.

XBR0\_CP1E\_\_ENABLED EQU 020H ; CP1 routed to Port pin.

XBR0\_CP1AE\_\_BMASK EQU 040H ; Comparator1 Asynchronous Output Enable

XBR0\_CP1AE\_\_SHIFT EQU 006H ; Comparator1 Asynchronous Output Enable

XBR0\_CP1AE\_\_DISABLED EQU 000H ; Asynchronous CP1 unavailable at Port pin.

XBR0\_CP1AE\_\_ENABLED EQU 040H ; Asynchronous CP1 routed to Port pin.

XBR0\_SYSCKE\_\_BMASK EQU 080H ; SYSCLK Output Enable

XBR0\_SYSCKE\_\_SHIFT EQU 007H ; SYSCLK Output Enable

XBR0\_SYSCKE\_\_DISABLED EQU 000H ; SYSCLK unavailable at Port pin.

XBR0\_SYSCKE\_\_ENABLED EQU 080H ; SYSCLK output routed to Port pin.

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; XBR1 Enums (Port I/O Crossbar 1 @ 0xE2)

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XBR1\_PCA0ME\_\_FMASK EQU 007H ; PCA Module I/O Enable

XBR1\_PCA0ME\_\_SHIFT EQU 000H ; PCA Module I/O Enable

XBR1\_PCA0ME\_\_DISABLED EQU 000H ; All PCA I/O unavailable at Port pins.

XBR1\_PCA0ME\_\_CEX0 EQU 001H ; CEX0 routed to Port pin.

XBR1\_PCA0ME\_\_CEX0\_TO\_CEX1 EQU 002H ; CEX0, CEX1 routed to Port pins.

XBR1\_PCA0ME\_\_CEX0\_TO\_CEX2 EQU 003H ; CEX0, CEX1, CEX2 routed to Port pins.

XBR1\_PCA0ME\_\_CEX0\_TO\_CEX3 EQU 004H ; CEX0, CEX1, CEX2, CEX3 routed to Port pins.

XBR1\_PCA0ME\_\_CEX0\_TO\_CEX4 EQU 005H ; CEX0, CEX1, CEX2, CEX3, CEX4 routed to Port pins.

XBR1\_PCA0ME\_\_CEX0\_TO\_CEX5 EQU 006H ; CEX0, CEX1, CEX2, CEX3, CEX4, CEX5 routed to Port

; pins.

XBR1\_ECIE\_\_BMASK EQU 008H ; PCA0 External Counter Input Enable

XBR1\_ECIE\_\_SHIFT EQU 003H ; PCA0 External Counter Input Enable

XBR1\_ECIE\_\_DISABLED EQU 000H ; ECI unavailable at Port pin.

XBR1\_ECIE\_\_ENABLED EQU 008H ; ECI routed to Port pin.

XBR1\_T0E\_\_BMASK EQU 010H ; T0 Enable

XBR1\_T0E\_\_SHIFT EQU 004H ; T0 Enable

XBR1\_T0E\_\_DISABLED EQU 000H ; T0 unavailable at Port pin.

XBR1\_T0E\_\_ENABLED EQU 010H ; T0 routed to Port pin.

XBR1\_T1E\_\_BMASK EQU 020H ; T1 Enable

XBR1\_T1E\_\_SHIFT EQU 005H ; T1 Enable

XBR1\_T1E\_\_DISABLED EQU 000H ; T1 unavailable at Port pin.

XBR1\_T1E\_\_ENABLED EQU 020H ; T1 routed to Port pin.

XBR1\_T2E\_\_BMASK EQU 040H ; T2 Enable

XBR1\_T2E\_\_SHIFT EQU 006H ; T2 Enable

XBR1\_T2E\_\_DISABLED EQU 000H ; T2 unavailable at Port pin.

XBR1\_T2E\_\_ENABLED EQU 040H ; T2 routed to Port pin.

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; XBR2 Enums (Port I/O Crossbar 2 @ 0xE3)

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XBR2\_URT1E\_\_BMASK EQU 001H ; UART1 I/O Enable

XBR2\_URT1E\_\_SHIFT EQU 000H ; UART1 I/O Enable

XBR2\_URT1E\_\_DISABLED EQU 000H ; UART1 I/O unavailable at Port pin.

XBR2\_URT1E\_\_ENABLED EQU 001H ; UART1 TX1 RX1 routed to Port pins.

XBR2\_URT1RTSE\_\_BMASK EQU 002H ; UART1 RTS Output Enable

XBR2\_URT1RTSE\_\_SHIFT EQU 001H ; UART1 RTS Output Enable

XBR2\_URT1RTSE\_\_DISABLED EQU 000H ; UART1 RTS1 unavailable at Port pin.

XBR2\_URT1RTSE\_\_ENABLED EQU 002H ; UART1 RTS1 routed to Port pin.

XBR2\_URT1CTSE\_\_BMASK EQU 004H ; UART1 CTS Input Enable

XBR2\_URT1CTSE\_\_SHIFT EQU 002H ; UART1 CTS Input Enable

XBR2\_URT1CTSE\_\_DISABLED EQU 000H ; UART1 CTS1 unavailable at Port pin.

XBR2\_URT1CTSE\_\_ENABLED EQU 004H ; UART1 CTS1 routed to Port pin.

XBR2\_XBARE\_\_BMASK EQU 040H ; Crossbar Enable

XBR2\_XBARE\_\_SHIFT EQU 006H ; Crossbar Enable

XBR2\_XBARE\_\_DISABLED EQU 000H ; Crossbar disabled.

XBR2\_XBARE\_\_ENABLED EQU 040H ; Crossbar enabled.

XBR2\_WEAKPUD\_\_BMASK EQU 080H ; Port I/O Weak Pullup Disable

XBR2\_WEAKPUD\_\_SHIFT EQU 007H ; Port I/O Weak Pullup Disable

XBR2\_WEAKPUD\_\_PULL\_UPS\_ENABLED EQU 000H ; Weak Pullups enabled (except for Ports whose I/O

; are configured for analog mode).

XBR2\_WEAKPUD\_\_PULL\_UPS\_DISABLED EQU 080H ; Weak Pullups disabled.

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; PCA0CPH0 Enums (PCA Channel 0 Capture Module High Byte @ 0xFC)

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PCA0CPH0\_PCA0CPH0\_\_FMASK EQU 0FFH ; PCA Channel 0 Capture Module High Byte

PCA0CPH0\_PCA0CPH0\_\_SHIFT EQU 000H ; PCA Channel 0 Capture Module High Byte

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; PCA0CPL0 Enums (PCA Channel 0 Capture Module Low Byte @ 0xFB)

;------------------------------------------------------------------------------

PCA0CPL0\_PCA0CPL0\_\_FMASK EQU 0FFH ; PCA Channel 0 Capture Module Low Byte

PCA0CPL0\_PCA0CPL0\_\_SHIFT EQU 000H ; PCA Channel 0 Capture Module Low Byte

;------------------------------------------------------------------------------

; PCA0CPM0 Enums (PCA Channel 0 Capture/Compare Mode @ 0xDA)

;------------------------------------------------------------------------------

PCA0CPM0\_ECCF\_\_BMASK EQU 001H ; Channel 0 Capture/Compare Flag Interrupt Enable

PCA0CPM0\_ECCF\_\_SHIFT EQU 000H ; Channel 0 Capture/Compare Flag Interrupt Enable

PCA0CPM0\_ECCF\_\_DISABLED EQU 000H ; Disable CCF0 interrupts.

PCA0CPM0\_ECCF\_\_ENABLED EQU 001H ; Enable a Capture/Compare Flag interrupt request

; when CCF0 is set.

PCA0CPM0\_PWM\_\_BMASK EQU 002H ; Channel 0 Pulse Width Modulation Mode Enable

PCA0CPM0\_PWM\_\_SHIFT EQU 001H ; Channel 0 Pulse Width Modulation Mode Enable

PCA0CPM0\_PWM\_\_DISABLED EQU 000H ; Disable PWM function.

PCA0CPM0\_PWM\_\_ENABLED EQU 002H ; Enable PWM function.

PCA0CPM0\_TOG\_\_BMASK EQU 004H ; Channel 0 Toggle Function Enable

PCA0CPM0\_TOG\_\_SHIFT EQU 002H ; Channel 0 Toggle Function Enable

PCA0CPM0\_TOG\_\_DISABLED EQU 000H ; Disable toggle function.

PCA0CPM0\_TOG\_\_ENABLED EQU 004H ; Enable toggle function.

PCA0CPM0\_MAT\_\_BMASK EQU 008H ; Channel 0 Match Function Enable

PCA0CPM0\_MAT\_\_SHIFT EQU 003H ; Channel 0 Match Function Enable

PCA0CPM0\_MAT\_\_DISABLED EQU 000H ; Disable match function.

PCA0CPM0\_MAT\_\_ENABLED EQU 008H ; Enable match function.

PCA0CPM0\_CAPN\_\_BMASK EQU 010H ; Channel 0 Capture Negative Function Enable

PCA0CPM0\_CAPN\_\_SHIFT EQU 004H ; Channel 0 Capture Negative Function Enable

PCA0CPM0\_CAPN\_\_DISABLED EQU 000H ; Disable negative edge capture.

PCA0CPM0\_CAPN\_\_ENABLED EQU 010H ; Enable negative edge capture.

PCA0CPM0\_CAPP\_\_BMASK EQU 020H ; Channel 0 Capture Positive Function Enable

PCA0CPM0\_CAPP\_\_SHIFT EQU 005H ; Channel 0 Capture Positive Function Enable

PCA0CPM0\_CAPP\_\_DISABLED EQU 000H ; Disable positive edge capture.

PCA0CPM0\_CAPP\_\_ENABLED EQU 020H ; Enable positive edge capture.

PCA0CPM0\_ECOM\_\_BMASK EQU 040H ; Channel 0 Comparator Function Enable

PCA0CPM0\_ECOM\_\_SHIFT EQU 006H ; Channel 0 Comparator Function Enable

PCA0CPM0\_ECOM\_\_DISABLED EQU 000H ; Disable comparator function.

PCA0CPM0\_ECOM\_\_ENABLED EQU 040H ; Enable comparator function.

PCA0CPM0\_PWM16\_\_BMASK EQU 080H ; Channel 0 16-bit Pulse Width Modulation Enable

PCA0CPM0\_PWM16\_\_SHIFT EQU 007H ; Channel 0 16-bit Pulse Width Modulation Enable

PCA0CPM0\_PWM16\_\_8\_BIT EQU 000H ; 8 to 11-bit PWM selected.

PCA0CPM0\_PWM16\_\_16\_BIT EQU 080H ; 16-bit PWM selected.

;------------------------------------------------------------------------------

; PCA0CPH1 Enums (PCA Channel 1 Capture Module High Byte @ 0xEA)

;------------------------------------------------------------------------------

PCA0CPH1\_PCA0CPH1\_\_FMASK EQU 0FFH ; PCA Channel 1 Capture Module High Byte

PCA0CPH1\_PCA0CPH1\_\_SHIFT EQU 000H ; PCA Channel 1 Capture Module High Byte

;------------------------------------------------------------------------------

; PCA0CPL1 Enums (PCA Channel 1 Capture Module Low Byte @ 0xE9)

;------------------------------------------------------------------------------

PCA0CPL1\_PCA0CPL1\_\_FMASK EQU 0FFH ; PCA Channel 1 Capture Module Low Byte

PCA0CPL1\_PCA0CPL1\_\_SHIFT EQU 000H ; PCA Channel 1 Capture Module Low Byte

;------------------------------------------------------------------------------

; PCA0CPM1 Enums (PCA Channel 1 Capture/Compare Mode @ 0xDB)

;------------------------------------------------------------------------------

PCA0CPM1\_ECCF\_\_BMASK EQU 001H ; Channel 1 Capture/Compare Flag Interrupt Enable

PCA0CPM1\_ECCF\_\_SHIFT EQU 000H ; Channel 1 Capture/Compare Flag Interrupt Enable

PCA0CPM1\_ECCF\_\_DISABLED EQU 000H ; Disable CCF1 interrupts.

PCA0CPM1\_ECCF\_\_ENABLED EQU 001H ; Enable a Capture/Compare Flag interrupt request

; when CCF1 is set.

PCA0CPM1\_PWM\_\_BMASK EQU 002H ; Channel 1 Pulse Width Modulation Mode Enable

PCA0CPM1\_PWM\_\_SHIFT EQU 001H ; Channel 1 Pulse Width Modulation Mode Enable

PCA0CPM1\_PWM\_\_DISABLED EQU 000H ; Disable PWM function.

PCA0CPM1\_PWM\_\_ENABLED EQU 002H ; Enable PWM function.

PCA0CPM1\_TOG\_\_BMASK EQU 004H ; Channel 1 Toggle Function Enable

PCA0CPM1\_TOG\_\_SHIFT EQU 002H ; Channel 1 Toggle Function Enable

PCA0CPM1\_TOG\_\_DISABLED EQU 000H ; Disable toggle function.

PCA0CPM1\_TOG\_\_ENABLED EQU 004H ; Enable toggle function.

PCA0CPM1\_MAT\_\_BMASK EQU 008H ; Channel 1 Match Function Enable

PCA0CPM1\_MAT\_\_SHIFT EQU 003H ; Channel 1 Match Function Enable

PCA0CPM1\_MAT\_\_DISABLED EQU 000H ; Disable match function.

PCA0CPM1\_MAT\_\_ENABLED EQU 008H ; Enable match function.

PCA0CPM1\_CAPN\_\_BMASK EQU 010H ; Channel 1 Capture Negative Function Enable

PCA0CPM1\_CAPN\_\_SHIFT EQU 004H ; Channel 1 Capture Negative Function Enable

PCA0CPM1\_CAPN\_\_DISABLED EQU 000H ; Disable negative edge capture.

PCA0CPM1\_CAPN\_\_ENABLED EQU 010H ; Enable negative edge capture.

PCA0CPM1\_CAPP\_\_BMASK EQU 020H ; Channel 1 Capture Positive Function Enable

PCA0CPM1\_CAPP\_\_SHIFT EQU 005H ; Channel 1 Capture Positive Function Enable

PCA0CPM1\_CAPP\_\_DISABLED EQU 000H ; Disable positive edge capture.

PCA0CPM1\_CAPP\_\_ENABLED EQU 020H ; Enable positive edge capture.

PCA0CPM1\_ECOM\_\_BMASK EQU 040H ; Channel 1 Comparator Function Enable

PCA0CPM1\_ECOM\_\_SHIFT EQU 006H ; Channel 1 Comparator Function Enable

PCA0CPM1\_ECOM\_\_DISABLED EQU 000H ; Disable comparator function.

PCA0CPM1\_ECOM\_\_ENABLED EQU 040H ; Enable comparator function.

PCA0CPM1\_PWM16\_\_BMASK EQU 080H ; Channel 1 16-bit Pulse Width Modulation Enable

PCA0CPM1\_PWM16\_\_SHIFT EQU 007H ; Channel 1 16-bit Pulse Width Modulation Enable

PCA0CPM1\_PWM16\_\_8\_BIT EQU 000H ; 8 to 11-bit PWM selected.

PCA0CPM1\_PWM16\_\_16\_BIT EQU 080H ; 16-bit PWM selected.

;------------------------------------------------------------------------------

; PCA0CPH2 Enums (PCA Channel 2 Capture Module High Byte @ 0xEC)

;------------------------------------------------------------------------------

PCA0CPH2\_PCA0CPH2\_\_FMASK EQU 0FFH ; PCA Channel 2 Capture Module High Byte

PCA0CPH2\_PCA0CPH2\_\_SHIFT EQU 000H ; PCA Channel 2 Capture Module High Byte

;------------------------------------------------------------------------------

; PCA0CPL2 Enums (PCA Channel 2 Capture Module Low Byte @ 0xEB)

;------------------------------------------------------------------------------

PCA0CPL2\_PCA0CPL2\_\_FMASK EQU 0FFH ; PCA Channel 2 Capture Module Low Byte

PCA0CPL2\_PCA0CPL2\_\_SHIFT EQU 000H ; PCA Channel 2 Capture Module Low Byte

;------------------------------------------------------------------------------

; PCA0CPM2 Enums (PCA Channel 2 Capture/Compare Mode @ 0xDC)

;------------------------------------------------------------------------------

PCA0CPM2\_ECCF\_\_BMASK EQU 001H ; Channel 2 Capture/Compare Flag Interrupt Enable

PCA0CPM2\_ECCF\_\_SHIFT EQU 000H ; Channel 2 Capture/Compare Flag Interrupt Enable

PCA0CPM2\_ECCF\_\_DISABLED EQU 000H ; Disable CCF2 interrupts.

PCA0CPM2\_ECCF\_\_ENABLED EQU 001H ; Enable a Capture/Compare Flag interrupt request

; when CCF2 is set.

PCA0CPM2\_PWM\_\_BMASK EQU 002H ; Channel 2 Pulse Width Modulation Mode Enable

PCA0CPM2\_PWM\_\_SHIFT EQU 001H ; Channel 2 Pulse Width Modulation Mode Enable

PCA0CPM2\_PWM\_\_DISABLED EQU 000H ; Disable PWM function.

PCA0CPM2\_PWM\_\_ENABLED EQU 002H ; Enable PWM function.

PCA0CPM2\_TOG\_\_BMASK EQU 004H ; Channel 2 Toggle Function Enable

PCA0CPM2\_TOG\_\_SHIFT EQU 002H ; Channel 2 Toggle Function Enable

PCA0CPM2\_TOG\_\_DISABLED EQU 000H ; Disable toggle function.

PCA0CPM2\_TOG\_\_ENABLED EQU 004H ; Enable toggle function.

PCA0CPM2\_MAT\_\_BMASK EQU 008H ; Channel 2 Match Function Enable

PCA0CPM2\_MAT\_\_SHIFT EQU 003H ; Channel 2 Match Function Enable

PCA0CPM2\_MAT\_\_DISABLED EQU 000H ; Disable match function.

PCA0CPM2\_MAT\_\_ENABLED EQU 008H ; Enable match function.

PCA0CPM2\_CAPN\_\_BMASK EQU 010H ; Channel 2 Capture Negative Function Enable

PCA0CPM2\_CAPN\_\_SHIFT EQU 004H ; Channel 2 Capture Negative Function Enable

PCA0CPM2\_CAPN\_\_DISABLED EQU 000H ; Disable negative edge capture.

PCA0CPM2\_CAPN\_\_ENABLED EQU 010H ; Enable negative edge capture.

PCA0CPM2\_CAPP\_\_BMASK EQU 020H ; Channel 2 Capture Positive Function Enable

PCA0CPM2\_CAPP\_\_SHIFT EQU 005H ; Channel 2 Capture Positive Function Enable

PCA0CPM2\_CAPP\_\_DISABLED EQU 000H ; Disable positive edge capture.

PCA0CPM2\_CAPP\_\_ENABLED EQU 020H ; Enable positive edge capture.

PCA0CPM2\_ECOM\_\_BMASK EQU 040H ; Channel 2 Comparator Function Enable

PCA0CPM2\_ECOM\_\_SHIFT EQU 006H ; Channel 2 Comparator Function Enable

PCA0CPM2\_ECOM\_\_DISABLED EQU 000H ; Disable comparator function.

PCA0CPM2\_ECOM\_\_ENABLED EQU 040H ; Enable comparator function.

PCA0CPM2\_PWM16\_\_BMASK EQU 080H ; Channel 2 16-bit Pulse Width Modulation Enable

PCA0CPM2\_PWM16\_\_SHIFT EQU 007H ; Channel 2 16-bit Pulse Width Modulation Enable

PCA0CPM2\_PWM16\_\_8\_BIT EQU 000H ; 8 to 11-bit PWM selected.

PCA0CPM2\_PWM16\_\_16\_BIT EQU 080H ; 16-bit PWM selected.

;------------------------------------------------------------------------------

; PCA0CPH3 Enums (PCA Channel 3 Capture Module High Byte @ 0xF5)

;------------------------------------------------------------------------------

PCA0CPH3\_PCA0CPH3\_\_FMASK EQU 0FFH ; PCA Channel 3 Capture Module High Byte

PCA0CPH3\_PCA0CPH3\_\_SHIFT EQU 000H ; PCA Channel 3 Capture Module High Byte

;------------------------------------------------------------------------------

; PCA0CPL3 Enums (PCA Channel 3 Capture Module Low Byte @ 0xF4)

;------------------------------------------------------------------------------

PCA0CPL3\_PCA0CPL3\_\_FMASK EQU 0FFH ; PCA Channel 3 Capture Module Low Byte

PCA0CPL3\_PCA0CPL3\_\_SHIFT EQU 000H ; PCA Channel 3 Capture Module Low Byte

;------------------------------------------------------------------------------

; PCA0CPM3 Enums (PCA Channel 3 Capture/Compare Mode @ 0xAE)

;------------------------------------------------------------------------------

PCA0CPM3\_ECCF\_\_BMASK EQU 001H ; Channel 3 Capture/Compare Flag Interrupt Enable

PCA0CPM3\_ECCF\_\_SHIFT EQU 000H ; Channel 3 Capture/Compare Flag Interrupt Enable

PCA0CPM3\_ECCF\_\_DISABLED EQU 000H ; Disable CCF3 interrupts.

PCA0CPM3\_ECCF\_\_ENABLED EQU 001H ; Enable a Capture/Compare Flag interrupt request

; when CCF3 is set.

PCA0CPM3\_PWM\_\_BMASK EQU 002H ; Channel 3 Pulse Width Modulation Mode Enable

PCA0CPM3\_PWM\_\_SHIFT EQU 001H ; Channel 3 Pulse Width Modulation Mode Enable

PCA0CPM3\_PWM\_\_DISABLED EQU 000H ; Disable PWM function.

PCA0CPM3\_PWM\_\_ENABLED EQU 002H ; Enable PWM function.

PCA0CPM3\_TOG\_\_BMASK EQU 004H ; Channel 3 Toggle Function Enable

PCA0CPM3\_TOG\_\_SHIFT EQU 002H ; Channel 3 Toggle Function Enable

PCA0CPM3\_TOG\_\_DISABLED EQU 000H ; Disable toggle function.

PCA0CPM3\_TOG\_\_ENABLED EQU 004H ; Enable toggle function.

PCA0CPM3\_MAT\_\_BMASK EQU 008H ; Channel 3 Match Function Enable

PCA0CPM3\_MAT\_\_SHIFT EQU 003H ; Channel 3 Match Function Enable

PCA0CPM3\_MAT\_\_DISABLED EQU 000H ; Disable match function.

PCA0CPM3\_MAT\_\_ENABLED EQU 008H ; Enable match function.

PCA0CPM3\_CAPN\_\_BMASK EQU 010H ; Channel 3 Capture Negative Function Enable

PCA0CPM3\_CAPN\_\_SHIFT EQU 004H ; Channel 3 Capture Negative Function Enable

PCA0CPM3\_CAPN\_\_DISABLED EQU 000H ; Disable negative edge capture.

PCA0CPM3\_CAPN\_\_ENABLED EQU 010H ; Enable negative edge capture.

PCA0CPM3\_CAPP\_\_BMASK EQU 020H ; Channel 3 Capture Positive Function Enable

PCA0CPM3\_CAPP\_\_SHIFT EQU 005H ; Channel 3 Capture Positive Function Enable

PCA0CPM3\_CAPP\_\_DISABLED EQU 000H ; Disable positive edge capture.

PCA0CPM3\_CAPP\_\_ENABLED EQU 020H ; Enable positive edge capture.

PCA0CPM3\_ECOM\_\_BMASK EQU 040H ; Channel 3 Comparator Function Enable

PCA0CPM3\_ECOM\_\_SHIFT EQU 006H ; Channel 3 Comparator Function Enable

PCA0CPM3\_ECOM\_\_DISABLED EQU 000H ; Disable comparator function.

PCA0CPM3\_ECOM\_\_ENABLED EQU 040H ; Enable comparator function.

PCA0CPM3\_PWM16\_\_BMASK EQU 080H ; Channel 3 16-bit Pulse Width Modulation Enable

PCA0CPM3\_PWM16\_\_SHIFT EQU 007H ; Channel 3 16-bit Pulse Width Modulation Enable

PCA0CPM3\_PWM16\_\_8\_BIT EQU 000H ; 8 to 11-bit PWM selected.

PCA0CPM3\_PWM16\_\_16\_BIT EQU 080H ; 16-bit PWM selected.

;------------------------------------------------------------------------------

; PCA0CPH4 Enums (PCA Channel 4 Capture Module High Byte @ 0x85)

;------------------------------------------------------------------------------

PCA0CPH4\_PCA0CPH4\_\_FMASK EQU 0FFH ; PCA Channel 4 Capture Module High Byte

PCA0CPH4\_PCA0CPH4\_\_SHIFT EQU 000H ; PCA Channel 4 Capture Module High Byte

;------------------------------------------------------------------------------

; PCA0CPL4 Enums (PCA Channel 4 Capture Module Low Byte @ 0x84)

;------------------------------------------------------------------------------

PCA0CPL4\_PCA0CPL4\_\_FMASK EQU 0FFH ; PCA Channel 4 Capture Module Low Byte

PCA0CPL4\_PCA0CPL4\_\_SHIFT EQU 000H ; PCA Channel 4 Capture Module Low Byte

;------------------------------------------------------------------------------

; PCA0CPM4 Enums (PCA Channel 4 Capture/Compare Mode @ 0xAF)

;------------------------------------------------------------------------------

PCA0CPM4\_ECCF\_\_BMASK EQU 001H ; Channel 4 Capture/Compare Flag Interrupt Enable

PCA0CPM4\_ECCF\_\_SHIFT EQU 000H ; Channel 4 Capture/Compare Flag Interrupt Enable

PCA0CPM4\_ECCF\_\_DISABLED EQU 000H ; Disable CCF4 interrupts.

PCA0CPM4\_ECCF\_\_ENABLED EQU 001H ; Enable a Capture/Compare Flag interrupt request

; when CCF4 is set.

PCA0CPM4\_PWM\_\_BMASK EQU 002H ; Channel 4 Pulse Width Modulation Mode Enable

PCA0CPM4\_PWM\_\_SHIFT EQU 001H ; Channel 4 Pulse Width Modulation Mode Enable

PCA0CPM4\_PWM\_\_DISABLED EQU 000H ; Disable PWM function.

PCA0CPM4\_PWM\_\_ENABLED EQU 002H ; Enable PWM function.

PCA0CPM4\_TOG\_\_BMASK EQU 004H ; Channel 4 Toggle Function Enable

PCA0CPM4\_TOG\_\_SHIFT EQU 002H ; Channel 4 Toggle Function Enable

PCA0CPM4\_TOG\_\_DISABLED EQU 000H ; Disable toggle function.

PCA0CPM4\_TOG\_\_ENABLED EQU 004H ; Enable toggle function.

PCA0CPM4\_MAT\_\_BMASK EQU 008H ; Channel 4 Match Function Enable

PCA0CPM4\_MAT\_\_SHIFT EQU 003H ; Channel 4 Match Function Enable

PCA0CPM4\_MAT\_\_DISABLED EQU 000H ; Disable match function.

PCA0CPM4\_MAT\_\_ENABLED EQU 008H ; Enable match function.

PCA0CPM4\_CAPN\_\_BMASK EQU 010H ; Channel 4 Capture Negative Function Enable

PCA0CPM4\_CAPN\_\_SHIFT EQU 004H ; Channel 4 Capture Negative Function Enable

PCA0CPM4\_CAPN\_\_DISABLED EQU 000H ; Disable negative edge capture.

PCA0CPM4\_CAPN\_\_ENABLED EQU 010H ; Enable negative edge capture.

PCA0CPM4\_CAPP\_\_BMASK EQU 020H ; Channel 4 Capture Positive Function Enable

PCA0CPM4\_CAPP\_\_SHIFT EQU 005H ; Channel 4 Capture Positive Function Enable

PCA0CPM4\_CAPP\_\_DISABLED EQU 000H ; Disable positive edge capture.

PCA0CPM4\_CAPP\_\_ENABLED EQU 020H ; Enable positive edge capture.

PCA0CPM4\_ECOM\_\_BMASK EQU 040H ; Channel 4 Comparator Function Enable

PCA0CPM4\_ECOM\_\_SHIFT EQU 006H ; Channel 4 Comparator Function Enable

PCA0CPM4\_ECOM\_\_DISABLED EQU 000H ; Disable comparator function.

PCA0CPM4\_ECOM\_\_ENABLED EQU 040H ; Enable comparator function.

PCA0CPM4\_PWM16\_\_BMASK EQU 080H ; Channel 4 16-bit Pulse Width Modulation Enable

PCA0CPM4\_PWM16\_\_SHIFT EQU 007H ; Channel 4 16-bit Pulse Width Modulation Enable

PCA0CPM4\_PWM16\_\_8\_BIT EQU 000H ; 8 to 11-bit PWM selected.

PCA0CPM4\_PWM16\_\_16\_BIT EQU 080H ; 16-bit PWM selected.

;------------------------------------------------------------------------------

; PCA0CPH5 Enums (PCA Channel 5 Capture Module High Byte @ 0xDE)

;------------------------------------------------------------------------------

PCA0CPH5\_PCA0CPH5\_\_FMASK EQU 0FFH ; PCA Channel 5 Capture Module High Byte

PCA0CPH5\_PCA0CPH5\_\_SHIFT EQU 000H ; PCA Channel 5 Capture Module High Byte

;------------------------------------------------------------------------------

; PCA0CPL5 Enums (PCA Channel 5 Capture Module Low Byte @ 0xDD)

;------------------------------------------------------------------------------

PCA0CPL5\_PCA0CPL5\_\_FMASK EQU 0FFH ; PCA Channel 5 Capture Module Low Byte

PCA0CPL5\_PCA0CPL5\_\_SHIFT EQU 000H ; PCA Channel 5 Capture Module Low Byte

;------------------------------------------------------------------------------

; PCA0CPM5 Enums (PCA Channel 5 Capture/Compare Mode @ 0xCC)

;------------------------------------------------------------------------------

PCA0CPM5\_ECCF\_\_BMASK EQU 001H ; Channel 5 Capture/Compare Flag Interrupt Enable

PCA0CPM5\_ECCF\_\_SHIFT EQU 000H ; Channel 5 Capture/Compare Flag Interrupt Enable

PCA0CPM5\_ECCF\_\_DISABLED EQU 000H ; Disable CCF5 interrupts.

PCA0CPM5\_ECCF\_\_ENABLED EQU 001H ; Enable a Capture/Compare Flag interrupt request

; when CCF5 is set.

PCA0CPM5\_PWM\_\_BMASK EQU 002H ; Channel 5 Pulse Width Modulation Mode Enable

PCA0CPM5\_PWM\_\_SHIFT EQU 001H ; Channel 5 Pulse Width Modulation Mode Enable

PCA0CPM5\_PWM\_\_DISABLED EQU 000H ; Disable PWM function.

PCA0CPM5\_PWM\_\_ENABLED EQU 002H ; Enable PWM function.

PCA0CPM5\_TOG\_\_BMASK EQU 004H ; Channel 5 Toggle Function Enable

PCA0CPM5\_TOG\_\_SHIFT EQU 002H ; Channel 5 Toggle Function Enable

PCA0CPM5\_TOG\_\_DISABLED EQU 000H ; Disable toggle function.

PCA0CPM5\_TOG\_\_ENABLED EQU 004H ; Enable toggle function.

PCA0CPM5\_MAT\_\_BMASK EQU 008H ; Channel 5 Match Function Enable

PCA0CPM5\_MAT\_\_SHIFT EQU 003H ; Channel 5 Match Function Enable

PCA0CPM5\_MAT\_\_DISABLED EQU 000H ; Disable match function.

PCA0CPM5\_MAT\_\_ENABLED EQU 008H ; Enable match function.

PCA0CPM5\_CAPN\_\_BMASK EQU 010H ; Channel 5 Capture Negative Function Enable

PCA0CPM5\_CAPN\_\_SHIFT EQU 004H ; Channel 5 Capture Negative Function Enable

PCA0CPM5\_CAPN\_\_DISABLED EQU 000H ; Disable negative edge capture.

PCA0CPM5\_CAPN\_\_ENABLED EQU 010H ; Enable negative edge capture.

PCA0CPM5\_CAPP\_\_BMASK EQU 020H ; Channel 5 Capture Positive Function Enable

PCA0CPM5\_CAPP\_\_SHIFT EQU 005H ; Channel 5 Capture Positive Function Enable

PCA0CPM5\_CAPP\_\_DISABLED EQU 000H ; Disable positive edge capture.

PCA0CPM5\_CAPP\_\_ENABLED EQU 020H ; Enable positive edge capture.

PCA0CPM5\_ECOM\_\_BMASK EQU 040H ; Channel 5 Comparator Function Enable

PCA0CPM5\_ECOM\_\_SHIFT EQU 006H ; Channel 5 Comparator Function Enable

PCA0CPM5\_ECOM\_\_DISABLED EQU 000H ; Disable comparator function.

PCA0CPM5\_ECOM\_\_ENABLED EQU 040H ; Enable comparator function.

PCA0CPM5\_PWM16\_\_BMASK EQU 080H ; Channel 5 16-bit Pulse Width Modulation Enable

PCA0CPM5\_PWM16\_\_SHIFT EQU 007H ; Channel 5 16-bit Pulse Width Modulation Enable

PCA0CPM5\_PWM16\_\_8\_BIT EQU 000H ; 8 to 11-bit PWM selected.

PCA0CPM5\_PWM16\_\_16\_BIT EQU 080H ; 16-bit PWM selected.

;------------------------------------------------------------------------------

; PCA0CENT Enums (PCA Center Alignment Enable @ 0x9E)

;------------------------------------------------------------------------------

PCA0CENT\_CEX0CEN\_\_BMASK EQU 001H ; CEX0 Center Alignment Enable

PCA0CENT\_CEX0CEN\_\_SHIFT EQU 000H ; CEX0 Center Alignment Enable

PCA0CENT\_CEX0CEN\_\_EDGE EQU 000H ; Edge-aligned.

PCA0CENT\_CEX0CEN\_\_CENTER EQU 001H ; Center-aligned.

PCA0CENT\_CEX1CEN\_\_BMASK EQU 002H ; CEX1 Center Alignment Enable

PCA0CENT\_CEX1CEN\_\_SHIFT EQU 001H ; CEX1 Center Alignment Enable

PCA0CENT\_CEX1CEN\_\_EDGE EQU 000H ; Edge-aligned.

PCA0CENT\_CEX1CEN\_\_CENTER EQU 002H ; Center-aligned.

PCA0CENT\_CEX2CEN\_\_BMASK EQU 004H ; CEX2 Center Alignment Enable

PCA0CENT\_CEX2CEN\_\_SHIFT EQU 002H ; CEX2 Center Alignment Enable

PCA0CENT\_CEX2CEN\_\_EDGE EQU 000H ; Edge-aligned.

PCA0CENT\_CEX2CEN\_\_CENTER EQU 004H ; Center-aligned.

PCA0CENT\_CEX3CEN\_\_BMASK EQU 008H ; CEX3 Center Alignment Enable

PCA0CENT\_CEX3CEN\_\_SHIFT EQU 003H ; CEX3 Center Alignment Enable

PCA0CENT\_CEX3CEN\_\_EDGE EQU 000H ; Edge-aligned.

PCA0CENT\_CEX3CEN\_\_CENTER EQU 008H ; Center-aligned.

PCA0CENT\_CEX4CEN\_\_BMASK EQU 010H ; CEX4 Center Alignment Enable

PCA0CENT\_CEX4CEN\_\_SHIFT EQU 004H ; CEX4 Center Alignment Enable

PCA0CENT\_CEX4CEN\_\_EDGE EQU 000H ; Edge-aligned.

PCA0CENT\_CEX4CEN\_\_CENTER EQU 010H ; Center-aligned.

PCA0CENT\_CEX5CEN\_\_BMASK EQU 020H ; CEX5 Center Alignment Enable

PCA0CENT\_CEX5CEN\_\_SHIFT EQU 005H ; CEX5 Center Alignment Enable

PCA0CENT\_CEX5CEN\_\_EDGE EQU 000H ; Edge-aligned.

PCA0CENT\_CEX5CEN\_\_CENTER EQU 020H ; Center-aligned.

;------------------------------------------------------------------------------

; PCA0CLR Enums (PCA Comparator Clear Control @ 0x9C)

;------------------------------------------------------------------------------

PCA0CLR\_CPCE0\_\_BMASK EQU 001H ; Comparator Clear Enable for CEX0

PCA0CLR\_CPCE0\_\_SHIFT EQU 000H ; Comparator Clear Enable for CEX0

PCA0CLR\_CPCE0\_\_DISABLED EQU 000H ; Disable the comparator clear function on PCA

; channel 0.

PCA0CLR\_CPCE0\_\_ENABLED EQU 001H ; Enable the comparator clear function on PCA

; channel 0.

PCA0CLR\_CPCE1\_\_BMASK EQU 002H ; Comparator Clear Enable for CEX1

PCA0CLR\_CPCE1\_\_SHIFT EQU 001H ; Comparator Clear Enable for CEX1

PCA0CLR\_CPCE1\_\_DISABLED EQU 000H ; Disable the comparator clear function on PCA

; channel 1.

PCA0CLR\_CPCE1\_\_ENABLED EQU 002H ; Enable the comparator clear function on PCA

; channel 1.

PCA0CLR\_CPCE2\_\_BMASK EQU 004H ; Comparator Clear Enable for CEX2

PCA0CLR\_CPCE2\_\_SHIFT EQU 002H ; Comparator Clear Enable for CEX2

PCA0CLR\_CPCE2\_\_DISABLED EQU 000H ; Disable the comparator clear function on PCA

; channel 2.

PCA0CLR\_CPCE2\_\_ENABLED EQU 004H ; Enable the comparator clear function on PCA

; channel 2.

PCA0CLR\_CPCE3\_\_BMASK EQU 008H ; Comparator Clear Enable for CEX3

PCA0CLR\_CPCE3\_\_SHIFT EQU 003H ; Comparator Clear Enable for CEX3

PCA0CLR\_CPCE3\_\_DISABLED EQU 000H ; Disable the comparator clear function on PCA

; channel 3.

PCA0CLR\_CPCE3\_\_ENABLED EQU 008H ; Enable the comparator clear function on PCA

; channel 3.

PCA0CLR\_CPCE4\_\_BMASK EQU 010H ; Comparator Clear Enable for CEX4

PCA0CLR\_CPCE4\_\_SHIFT EQU 004H ; Comparator Clear Enable for CEX4

PCA0CLR\_CPCE4\_\_DISABLED EQU 000H ; Disable the comparator clear function on PCA

; channel 4.

PCA0CLR\_CPCE4\_\_ENABLED EQU 010H ; Enable the comparator clear function on PCA

; channel 4.

PCA0CLR\_CPCE5\_\_BMASK EQU 020H ; Comparator Clear Enable for CEX5

PCA0CLR\_CPCE5\_\_SHIFT EQU 005H ; Comparator Clear Enable for CEX5

PCA0CLR\_CPCE5\_\_DISABLED EQU 000H ; Disable the comparator clear function on PCA

; channel 5.

PCA0CLR\_CPCE5\_\_ENABLED EQU 020H ; Enable the comparator clear function on PCA

; channel 5.

PCA0CLR\_CPCSEL\_\_BMASK EQU 040H ; Comparator Clear Select

PCA0CLR\_CPCSEL\_\_SHIFT EQU 006H ; Comparator Clear Select

PCA0CLR\_CPCSEL\_\_CMP\_0 EQU 000H ; Comparator 0 will be used for the comparator clear

; function.

PCA0CLR\_CPCSEL\_\_CMP\_1 EQU 040H ; Comparator 1 will be used for the comparator clear

; function.

PCA0CLR\_CPCPOL\_\_BMASK EQU 080H ; Comparator Clear Polarity

PCA0CLR\_CPCPOL\_\_SHIFT EQU 007H ; Comparator Clear Polarity

PCA0CLR\_CPCPOL\_\_LOW EQU 000H ; PCA channel(s) will be cleared when comparator

; result goes logic low.

PCA0CLR\_CPCPOL\_\_HIGH EQU 080H ; PCA channel(s) will be cleared when comparator

; result goes logic high.

;------------------------------------------------------------------------------

; PCA0CN0 Enums (PCA Control @ 0xD8)

;------------------------------------------------------------------------------

PCA0CN0\_CCF0\_\_BMASK EQU 001H ; PCA Module 0 Capture/Compare Flag

PCA0CN0\_CCF0\_\_SHIFT EQU 000H ; PCA Module 0 Capture/Compare Flag

PCA0CN0\_CCF0\_\_NOT\_SET EQU 000H ; A match or capture did not occur on channel 0.

PCA0CN0\_CCF0\_\_SET EQU 001H ; A match or capture occurred on channel 0.

PCA0CN0\_CCF1\_\_BMASK EQU 002H ; PCA Module 1 Capture/Compare Flag

PCA0CN0\_CCF1\_\_SHIFT EQU 001H ; PCA Module 1 Capture/Compare Flag

PCA0CN0\_CCF1\_\_NOT\_SET EQU 000H ; A match or capture did not occur on channel 1.

PCA0CN0\_CCF1\_\_SET EQU 002H ; A match or capture occurred on channel 1.

PCA0CN0\_CCF2\_\_BMASK EQU 004H ; PCA Module 2 Capture/Compare Flag

PCA0CN0\_CCF2\_\_SHIFT EQU 002H ; PCA Module 2 Capture/Compare Flag

PCA0CN0\_CCF2\_\_NOT\_SET EQU 000H ; A match or capture did not occur on channel 2.

PCA0CN0\_CCF2\_\_SET EQU 004H ; A match or capture occurred on channel 2.

PCA0CN0\_CCF3\_\_BMASK EQU 008H ; PCA Module 3 Capture/Compare Flag

PCA0CN0\_CCF3\_\_SHIFT EQU 003H ; PCA Module 3 Capture/Compare Flag

PCA0CN0\_CCF3\_\_NOT\_SET EQU 000H ; A match or capture did not occur on channel 3.

PCA0CN0\_CCF3\_\_SET EQU 008H ; A match or capture occurred on channel 3.

PCA0CN0\_CCF4\_\_BMASK EQU 010H ; PCA Module 4 Capture/Compare Flag

PCA0CN0\_CCF4\_\_SHIFT EQU 004H ; PCA Module 4 Capture/Compare Flag

PCA0CN0\_CCF4\_\_NOT\_SET EQU 000H ; A match or capture did not occur on channel 4.

PCA0CN0\_CCF4\_\_SET EQU 010H ; A match or capture occurred on channel 4.

PCA0CN0\_CCF5\_\_BMASK EQU 020H ; PCA Module 5 Capture/Compare Flag

PCA0CN0\_CCF5\_\_SHIFT EQU 005H ; PCA Module 5 Capture/Compare Flag

PCA0CN0\_CCF5\_\_NOT\_SET EQU 000H ; A match or capture did not occur on channel 5.

PCA0CN0\_CCF5\_\_SET EQU 020H ; A match or capture occurred on channel 5.

PCA0CN0\_CR\_\_BMASK EQU 040H ; PCA Counter/Timer Run Control

PCA0CN0\_CR\_\_SHIFT EQU 006H ; PCA Counter/Timer Run Control

PCA0CN0\_CR\_\_STOP EQU 000H ; Stop the PCA Counter/Timer.

PCA0CN0\_CR\_\_RUN EQU 040H ; Start the PCA Counter/Timer running.

PCA0CN0\_CF\_\_BMASK EQU 080H ; PCA Counter/Timer Overflow Flag

PCA0CN0\_CF\_\_SHIFT EQU 007H ; PCA Counter/Timer Overflow Flag

PCA0CN0\_CF\_\_NOT\_SET EQU 000H ; The PCA counter/timer did not overflow.

PCA0CN0\_CF\_\_SET EQU 080H ; The PCA counter/timer overflowed.

;------------------------------------------------------------------------------

; PCA0H Enums (PCA Counter/Timer High Byte @ 0xFA)

;------------------------------------------------------------------------------

PCA0H\_PCA0H\_\_FMASK EQU 0FFH ; PCA Counter/Timer High Byte

PCA0H\_PCA0H\_\_SHIFT EQU 000H ; PCA Counter/Timer High Byte

;------------------------------------------------------------------------------

; PCA0L Enums (PCA Counter/Timer Low Byte @ 0xF9)

;------------------------------------------------------------------------------

PCA0L\_PCA0L\_\_FMASK EQU 0FFH ; PCA Counter/Timer Low Byte

PCA0L\_PCA0L\_\_SHIFT EQU 000H ; PCA Counter/Timer Low Byte

;------------------------------------------------------------------------------

; PCA0MD Enums (PCA Mode @ 0xD9)

;------------------------------------------------------------------------------

PCA0MD\_ECF\_\_BMASK EQU 001H ; PCA Counter/Timer Overflow Interrupt Enable

PCA0MD\_ECF\_\_SHIFT EQU 000H ; PCA Counter/Timer Overflow Interrupt Enable

PCA0MD\_ECF\_\_OVF\_INT\_DISABLED EQU 000H ; Disable the CF interrupt.

PCA0MD\_ECF\_\_OVF\_INT\_ENABLED EQU 001H ; Enable a PCA Counter/Timer Overflow interrupt

; request when CF is set.

PCA0MD\_CPS\_\_FMASK EQU 00EH ; PCA Counter/Timer Pulse Select

PCA0MD\_CPS\_\_SHIFT EQU 001H ; PCA Counter/Timer Pulse Select

PCA0MD\_CPS\_\_SYSCLK\_DIV\_12 EQU 000H ; System clock divided by 12.

PCA0MD\_CPS\_\_SYSCLK\_DIV\_4 EQU 002H ; System clock divided by 4.

PCA0MD\_CPS\_\_T0\_OVERFLOW EQU 004H ; Timer 0 overflow.

PCA0MD\_CPS\_\_ECI EQU 006H ; High-to-low transitions on ECI (max rate = system

; clock divided by 4).

PCA0MD\_CPS\_\_SYSCLK EQU 008H ; System clock.

PCA0MD\_CPS\_\_EXTOSC\_DIV\_8 EQU 00AH ; External clock divided by 8 (synchronized with the

; system clock).

PCA0MD\_CPS\_\_LFOSC\_DIV\_8 EQU 00CH ; Low frequency oscillator divided by 8.

PCA0MD\_CIDL\_\_BMASK EQU 080H ; PCA Counter/Timer Idle Control

PCA0MD\_CIDL\_\_SHIFT EQU 007H ; PCA Counter/Timer Idle Control

PCA0MD\_CIDL\_\_NORMAL EQU 000H ; PCA continues to function normally while the

; system controller is in Idle Mode.

PCA0MD\_CIDL\_\_SUSPEND EQU 080H ; PCA operation is suspended while the system

; controller is in Idle Mode.

;------------------------------------------------------------------------------

; PCA0POL Enums (PCA Output Polarity @ 0x96)

;------------------------------------------------------------------------------

PCA0POL\_CEX0POL\_\_BMASK EQU 001H ; CEX0 Output Polarity

PCA0POL\_CEX0POL\_\_SHIFT EQU 000H ; CEX0 Output Polarity

PCA0POL\_CEX0POL\_\_DEFAULT EQU 000H ; Use default polarity.

PCA0POL\_CEX0POL\_\_INVERT EQU 001H ; Invert polarity.

PCA0POL\_CEX1POL\_\_BMASK EQU 002H ; CEX1 Output Polarity

PCA0POL\_CEX1POL\_\_SHIFT EQU 001H ; CEX1 Output Polarity

PCA0POL\_CEX1POL\_\_DEFAULT EQU 000H ; Use default polarity.

PCA0POL\_CEX1POL\_\_INVERT EQU 002H ; Invert polarity.

PCA0POL\_CEX2POL\_\_BMASK EQU 004H ; CEX2 Output Polarity

PCA0POL\_CEX2POL\_\_SHIFT EQU 002H ; CEX2 Output Polarity

PCA0POL\_CEX2POL\_\_DEFAULT EQU 000H ; Use default polarity.

PCA0POL\_CEX2POL\_\_INVERT EQU 004H ; Invert polarity.

PCA0POL\_CEX3POL\_\_BMASK EQU 008H ; CEX3 Output Polarity

PCA0POL\_CEX3POL\_\_SHIFT EQU 003H ; CEX3 Output Polarity

PCA0POL\_CEX3POL\_\_DEFAULT EQU 000H ; Use default polarity.

PCA0POL\_CEX3POL\_\_INVERT EQU 008H ; Invert polarity.

PCA0POL\_CEX4POL\_\_BMASK EQU 010H ; CEX4 Output Polarity

PCA0POL\_CEX4POL\_\_SHIFT EQU 004H ; CEX4 Output Polarity

PCA0POL\_CEX4POL\_\_DEFAULT EQU 000H ; Use default polarity.

PCA0POL\_CEX4POL\_\_INVERT EQU 010H ; Invert polarity.

PCA0POL\_CEX5POL\_\_BMASK EQU 020H ; CEX5 Output Polarity

PCA0POL\_CEX5POL\_\_SHIFT EQU 005H ; CEX5 Output Polarity

PCA0POL\_CEX5POL\_\_DEFAULT EQU 000H ; Use default polarity.

PCA0POL\_CEX5POL\_\_INVERT EQU 020H ; Invert polarity.

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; PCA0PWM Enums (PCA PWM Configuration @ 0xF7)

;------------------------------------------------------------------------------

PCA0PWM\_CLSEL\_\_FMASK EQU 007H ; Cycle Length Select

PCA0PWM\_CLSEL\_\_SHIFT EQU 000H ; Cycle Length Select

PCA0PWM\_CLSEL\_\_8\_BITS EQU 000H ; 8 bits.

PCA0PWM\_CLSEL\_\_9\_BITS EQU 001H ; 9 bits.

PCA0PWM\_CLSEL\_\_10\_BITS EQU 002H ; 10 bits.

PCA0PWM\_CLSEL\_\_11\_BITS EQU 003H ; 11 bits.

PCA0PWM\_COVF\_\_BMASK EQU 020H ; Cycle Overflow Flag

PCA0PWM\_COVF\_\_SHIFT EQU 005H ; Cycle Overflow Flag

PCA0PWM\_COVF\_\_NO\_OVERFLOW EQU 000H ; No overflow has occurred since the last time this

; bit was cleared.

PCA0PWM\_COVF\_\_OVERFLOW EQU 020H ; An overflow has occurred since the last time this

; bit was cleared.

PCA0PWM\_ECOV\_\_BMASK EQU 040H ; Cycle Overflow Interrupt Enable

PCA0PWM\_ECOV\_\_SHIFT EQU 006H ; Cycle Overflow Interrupt Enable

PCA0PWM\_ECOV\_\_COVF\_MASK\_DISABLED EQU 000H ; COVF will not generate PCA interrupts.

PCA0PWM\_ECOV\_\_COVF\_MASK\_ENABLED EQU 040H ; A PCA interrupt will be generated when COVF is

; set.

PCA0PWM\_ARSEL\_\_BMASK EQU 080H ; Auto-Reload Register Select

PCA0PWM\_ARSEL\_\_SHIFT EQU 007H ; Auto-Reload Register Select

PCA0PWM\_ARSEL\_\_CAPTURE\_COMPARE EQU 000H ; Read/Write Capture/Compare Registers at PCA0CPHn

; and PCA0CPLn.

PCA0PWM\_ARSEL\_\_AUTORELOAD EQU 080H ; Read/Write Auto-Reload Registers at PCA0CPHn and

; PCA0CPLn.

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; PCON0 Enums (Power Control @ 0x87)

;------------------------------------------------------------------------------

PCON0\_IDLE\_\_BMASK EQU 001H ; Idle Mode Select

PCON0\_IDLE\_\_SHIFT EQU 000H ; Idle Mode Select

PCON0\_IDLE\_\_NORMAL EQU 000H ; Idle mode not activated.

PCON0\_IDLE\_\_IDLE EQU 001H ; CPU goes into Idle mode (shuts off clock to CPU,

; but clocks to enabled peripherals are still

; active).

PCON0\_STOP\_\_BMASK EQU 002H ; Stop Mode Select

PCON0\_STOP\_\_SHIFT EQU 001H ; Stop Mode Select

PCON0\_STOP\_\_NORMAL EQU 000H ; Stop mode not activated.

PCON0\_STOP\_\_STOP EQU 002H ; CPU goes into Stop mode (internal oscillator

; stopped).

PCON0\_GF0\_\_BMASK EQU 004H ; General Purpose Flag 0

PCON0\_GF0\_\_SHIFT EQU 002H ; General Purpose Flag 0

PCON0\_GF0\_\_NOT\_SET EQU 000H ; The GF0 flag is not set. Clear the GF0 flag.

PCON0\_GF0\_\_SET EQU 004H ; The GF0 flag is set. Set the GF0 flag.

PCON0\_GF1\_\_BMASK EQU 008H ; General Purpose Flag 1

PCON0\_GF1\_\_SHIFT EQU 003H ; General Purpose Flag 1

PCON0\_GF1\_\_NOT\_SET EQU 000H ; The GF1 flag is not set. Clear the GF1 flag.

PCON0\_GF1\_\_SET EQU 008H ; The GF1 flag is set. Set the GF1 flag.

PCON0\_GF2\_\_BMASK EQU 010H ; General Purpose Flag 2

PCON0\_GF2\_\_SHIFT EQU 004H ; General Purpose Flag 2

PCON0\_GF2\_\_NOT\_SET EQU 000H ; The GF2 flag is not set. Clear the GF2 flag.

PCON0\_GF2\_\_SET EQU 010H ; The GF2 flag is set. Set the GF2 flag.

PCON0\_GF3\_\_BMASK EQU 020H ; General Purpose Flag 3

PCON0\_GF3\_\_SHIFT EQU 005H ; General Purpose Flag 3

PCON0\_GF3\_\_NOT\_SET EQU 000H ; The GF3 flag is not set. Clear the GF3 flag.

PCON0\_GF3\_\_SET EQU 020H ; The GF3 flag is set. Set the GF3 flag.

PCON0\_GF4\_\_BMASK EQU 040H ; General Purpose Flag 4

PCON0\_GF4\_\_SHIFT EQU 006H ; General Purpose Flag 4

PCON0\_GF4\_\_NOT\_SET EQU 000H ; The GF4 flag is not set. Clear the GF4 flag.

PCON0\_GF4\_\_SET EQU 040H ; The GF4 flag is set. Set the GF4 flag.

PCON0\_GF5\_\_BMASK EQU 080H ; General Purpose Flag 5

PCON0\_GF5\_\_SHIFT EQU 007H ; General Purpose Flag 5

PCON0\_GF5\_\_NOT\_SET EQU 000H ; The GF5 flag is not set. Clear the GF5 flag.

PCON0\_GF5\_\_SET EQU 080H ; The GF5 flag is set. Set the GF5 flag.

;------------------------------------------------------------------------------

; PCON1 Enums (Power Control 1 @ 0xCD)

;------------------------------------------------------------------------------

PCON1\_PINRSTMD\_\_BMASK EQU 001H ; Pin Reset Mode

PCON1\_PINRSTMD\_\_SHIFT EQU 000H ; Pin Reset Mode

PCON1\_PINRSTMD\_\_RESET EQU 000H ; GPIO logic is reset when any reset event is

; asserted.

PCON1\_PINRSTMD\_\_RETAIN EQU 001H ; Pins will retain state across any reset except for

; power-on-reset events. Note that although pin

; configurations are maintained, the values of the

; pin control registers are reset. Registers PnMDIN,

; PnMDOUT, Pn, and the XBARE bit may not reflect the

; actual pin configuration at this time. New values

; written to these registers will take effect upon

; the write event.

PCON1\_SUSPEND\_\_BMASK EQU 040H ; Suspend Mode Select

PCON1\_SUSPEND\_\_SHIFT EQU 006H ; Suspend Mode Select

PCON1\_SUSPEND\_\_NORMAL EQU 000H ; Suspend mode not activated.

PCON1\_SUSPEND\_\_SUSPEND EQU 040H ; Device goes into suspend mode (high-frequency

; oscillators and SYSCLK are halted).

PCON1\_SNOOZE\_\_BMASK EQU 080H ; Snooze Mode Select

PCON1\_SNOOZE\_\_SHIFT EQU 007H ; Snooze Mode Select

PCON1\_SNOOZE\_\_NORMAL EQU 000H ; Snooze mode not activated.

PCON1\_SNOOZE\_\_SNOOZE EQU 080H ; Device goes into snooze mode (high-frequency

; oscillators and SYSCLK are halted, internal LDO in

; low-power state).

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; PSTAT0 Enums (PMU Status 0 @ 0xAA)

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PSTAT0\_CPT0WK\_\_BMASK EQU 001H ; Comparator 0 Wake Flag

PSTAT0\_CPT0WK\_\_SHIFT EQU 000H ; Comparator 0 Wake Flag

PSTAT0\_PMATWK\_\_BMASK EQU 002H ; Port Match Wake Flag

PSTAT0\_PMATWK\_\_SHIFT EQU 001H ; Port Match Wake Flag

PSTAT0\_TMR4WK\_\_BMASK EQU 004H ; Timer 4 Wake Flag

PSTAT0\_TMR4WK\_\_SHIFT EQU 002H ; Timer 4 Wake Flag

PSTAT0\_I2C0WK\_\_BMASK EQU 008H ; I2C0 Slave Wake Flag

PSTAT0\_I2C0WK\_\_SHIFT EQU 003H ; I2C0 Slave Wake Flag

PSTAT0\_SPI0WK\_\_BMASK EQU 010H ; SPI0 Slave Wake Flag

PSTAT0\_SPI0WK\_\_SHIFT EQU 004H ; SPI0 Slave Wake Flag

PSTAT0\_CL0WK\_\_BMASK EQU 020H ; Configurable Logic Wake Flag

PSTAT0\_CL0WK\_\_SHIFT EQU 005H ; Configurable Logic Wake Flag

;------------------------------------------------------------------------------

; P0 Enums (Port 0 Pin Latch @ 0x80)

;------------------------------------------------------------------------------

P0\_B0\_\_BMASK EQU 001H ; Port 0 Bit 0 Latch

P0\_B0\_\_SHIFT EQU 000H ; Port 0 Bit 0 Latch

P0\_B0\_\_LOW EQU 000H ; P0.0 is low. Set P0.0 to drive low.

P0\_B0\_\_HIGH EQU 001H ; P0.0 is high. Set P0.0 to drive or float high.

P0\_B1\_\_BMASK EQU 002H ; Port 0 Bit 1 Latch

P0\_B1\_\_SHIFT EQU 001H ; Port 0 Bit 1 Latch

P0\_B1\_\_LOW EQU 000H ; P0.1 is low. Set P0.1 to drive low.

P0\_B1\_\_HIGH EQU 002H ; P0.1 is high. Set P0.1 to drive or float high.

P0\_B2\_\_BMASK EQU 004H ; Port 0 Bit 2 Latch

P0\_B2\_\_SHIFT EQU 002H ; Port 0 Bit 2 Latch

P0\_B2\_\_LOW EQU 000H ; P0.2 is low. Set P0.2 to drive low.

P0\_B2\_\_HIGH EQU 004H ; P0.2 is high. Set P0.2 to drive or float high.

P0\_B3\_\_BMASK EQU 008H ; Port 0 Bit 3 Latch

P0\_B3\_\_SHIFT EQU 003H ; Port 0 Bit 3 Latch

P0\_B3\_\_LOW EQU 000H ; P0.3 is low. Set P0.3 to drive low.

P0\_B3\_\_HIGH EQU 008H ; P0.3 is high. Set P0.3 to drive or float high.

P0\_B4\_\_BMASK EQU 010H ; Port 0 Bit 4 Latch

P0\_B4\_\_SHIFT EQU 004H ; Port 0 Bit 4 Latch

P0\_B4\_\_LOW EQU 000H ; P0.4 is low. Set P0.4 to drive low.

P0\_B4\_\_HIGH EQU 010H ; P0.4 is high. Set P0.4 to drive or float high.

P0\_B5\_\_BMASK EQU 020H ; Port 0 Bit 5 Latch

P0\_B5\_\_SHIFT EQU 005H ; Port 0 Bit 5 Latch

P0\_B5\_\_LOW EQU 000H ; P0.5 is low. Set P0.5 to drive low.

P0\_B5\_\_HIGH EQU 020H ; P0.5 is high. Set P0.5 to drive or float high.

P0\_B6\_\_BMASK EQU 040H ; Port 0 Bit 6 Latch

P0\_B6\_\_SHIFT EQU 006H ; Port 0 Bit 6 Latch

P0\_B6\_\_LOW EQU 000H ; P0.6 is low. Set P0.6 to drive low.

P0\_B6\_\_HIGH EQU 040H ; P0.6 is high. Set P0.6 to drive or float high.

P0\_B7\_\_BMASK EQU 080H ; Port 0 Bit 7 Latch

P0\_B7\_\_SHIFT EQU 007H ; Port 0 Bit 7 Latch

P0\_B7\_\_LOW EQU 000H ; P0.7 is low. Set P0.7 to drive low.

P0\_B7\_\_HIGH EQU 080H ; P0.7 is high. Set P0.7 to drive or float high.

;------------------------------------------------------------------------------

; P0MASK Enums (Port 0 Mask @ 0xFE)

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P0MASK\_B0\_\_BMASK EQU 001H ; Port 0 Bit 0 Mask Value

P0MASK\_B0\_\_SHIFT EQU 000H ; Port 0 Bit 0 Mask Value

P0MASK\_B0\_\_IGNORED EQU 000H ; P0.0 pin logic value is ignored and will not cause

; a port mismatch event.

P0MASK\_B0\_\_COMPARED EQU 001H ; P0.0 pin logic value is compared to P0MAT.0.

P0MASK\_B1\_\_BMASK EQU 002H ; Port 0 Bit 1 Mask Value

P0MASK\_B1\_\_SHIFT EQU 001H ; Port 0 Bit 1 Mask Value

P0MASK\_B1\_\_IGNORED EQU 000H ; P0.1 pin logic value is ignored and will not cause

; a port mismatch event.

P0MASK\_B1\_\_COMPARED EQU 002H ; P0.1 pin logic value is compared to P0MAT.1.

P0MASK\_B2\_\_BMASK EQU 004H ; Port 0 Bit 2 Mask Value

P0MASK\_B2\_\_SHIFT EQU 002H ; Port 0 Bit 2 Mask Value

P0MASK\_B2\_\_IGNORED EQU 000H ; P0.2 pin logic value is ignored and will not cause

; a port mismatch event.

P0MASK\_B2\_\_COMPARED EQU 004H ; P0.2 pin logic value is compared to P0MAT.2.

P0MASK\_B3\_\_BMASK EQU 008H ; Port 0 Bit 3 Mask Value

P0MASK\_B3\_\_SHIFT EQU 003H ; Port 0 Bit 3 Mask Value

P0MASK\_B3\_\_IGNORED EQU 000H ; P0.3 pin logic value is ignored and will not cause

; a port mismatch event.

P0MASK\_B3\_\_COMPARED EQU 008H ; P0.3 pin logic value is compared to P0MAT.3.

P0MASK\_B4\_\_BMASK EQU 010H ; Port 0 Bit 4 Mask Value

P0MASK\_B4\_\_SHIFT EQU 004H ; Port 0 Bit 4 Mask Value

P0MASK\_B4\_\_IGNORED EQU 000H ; P0.4 pin logic value is ignored and will not cause

; a port mismatch event.

P0MASK\_B4\_\_COMPARED EQU 010H ; P0.4 pin logic value is compared to P0MAT.4.

P0MASK\_B5\_\_BMASK EQU 020H ; Port 0 Bit 5 Mask Value

P0MASK\_B5\_\_SHIFT EQU 005H ; Port 0 Bit 5 Mask Value

P0MASK\_B5\_\_IGNORED EQU 000H ; P0.5 pin logic value is ignored and will not cause

; a port mismatch event.

P0MASK\_B5\_\_COMPARED EQU 020H ; P0.5 pin logic value is compared to P0MAT.5.

P0MASK\_B6\_\_BMASK EQU 040H ; Port 0 Bit 6 Mask Value

P0MASK\_B6\_\_SHIFT EQU 006H ; Port 0 Bit 6 Mask Value

P0MASK\_B6\_\_IGNORED EQU 000H ; P0.6 pin logic value is ignored and will not cause

; a port mismatch event.

P0MASK\_B6\_\_COMPARED EQU 040H ; P0.6 pin logic value is compared to P0MAT.6.

P0MASK\_B7\_\_BMASK EQU 080H ; Port 0 Bit 7 Mask Value

P0MASK\_B7\_\_SHIFT EQU 007H ; Port 0 Bit 7 Mask Value

P0MASK\_B7\_\_IGNORED EQU 000H ; P0.7 pin logic value is ignored and will not cause

; a port mismatch event.

P0MASK\_B7\_\_COMPARED EQU 080H ; P0.7 pin logic value is compared to P0MAT.7.

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; P0MAT Enums (Port 0 Match @ 0xFD)

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P0MAT\_B0\_\_BMASK EQU 001H ; Port 0 Bit 0 Match Value

P0MAT\_B0\_\_SHIFT EQU 000H ; Port 0 Bit 0 Match Value

P0MAT\_B0\_\_LOW EQU 000H ; P0.0 pin logic value is compared with logic LOW.

P0MAT\_B0\_\_HIGH EQU 001H ; P0.0 pin logic value is compared with logic HIGH.

P0MAT\_B1\_\_BMASK EQU 002H ; Port 0 Bit 1 Match Value

P0MAT\_B1\_\_SHIFT EQU 001H ; Port 0 Bit 1 Match Value

P0MAT\_B1\_\_LOW EQU 000H ; P0.1 pin logic value is compared with logic LOW.

P0MAT\_B1\_\_HIGH EQU 002H ; P0.1 pin logic value is compared with logic HIGH.

P0MAT\_B2\_\_BMASK EQU 004H ; Port 0 Bit 2 Match Value

P0MAT\_B2\_\_SHIFT EQU 002H ; Port 0 Bit 2 Match Value

P0MAT\_B2\_\_LOW EQU 000H ; P0.2 pin logic value is compared with logic LOW.

P0MAT\_B2\_\_HIGH EQU 004H ; P0.2 pin logic value is compared with logic HIGH.

P0MAT\_B3\_\_BMASK EQU 008H ; Port 0 Bit 3 Match Value

P0MAT\_B3\_\_SHIFT EQU 003H ; Port 0 Bit 3 Match Value

P0MAT\_B3\_\_LOW EQU 000H ; P0.3 pin logic value is compared with logic LOW.

P0MAT\_B3\_\_HIGH EQU 008H ; P0.3 pin logic value is compared with logic HIGH.

P0MAT\_B4\_\_BMASK EQU 010H ; Port 0 Bit 4 Match Value

P0MAT\_B4\_\_SHIFT EQU 004H ; Port 0 Bit 4 Match Value

P0MAT\_B4\_\_LOW EQU 000H ; P0.4 pin logic value is compared with logic LOW.

P0MAT\_B4\_\_HIGH EQU 010H ; P0.4 pin logic value is compared with logic HIGH.

P0MAT\_B5\_\_BMASK EQU 020H ; Port 0 Bit 5 Match Value

P0MAT\_B5\_\_SHIFT EQU 005H ; Port 0 Bit 5 Match Value

P0MAT\_B5\_\_LOW EQU 000H ; P0.5 pin logic value is compared with logic LOW.

P0MAT\_B5\_\_HIGH EQU 020H ; P0.5 pin logic value is compared with logic HIGH.

P0MAT\_B6\_\_BMASK EQU 040H ; Port 0 Bit 6 Match Value

P0MAT\_B6\_\_SHIFT EQU 006H ; Port 0 Bit 6 Match Value

P0MAT\_B6\_\_LOW EQU 000H ; P0.6 pin logic value is compared with logic LOW.

P0MAT\_B6\_\_HIGH EQU 040H ; P0.6 pin logic value is compared with logic HIGH.

P0MAT\_B7\_\_BMASK EQU 080H ; Port 0 Bit 7 Match Value

P0MAT\_B7\_\_SHIFT EQU 007H ; Port 0 Bit 7 Match Value

P0MAT\_B7\_\_LOW EQU 000H ; P0.7 pin logic value is compared with logic LOW.

P0MAT\_B7\_\_HIGH EQU 080H ; P0.7 pin logic value is compared with logic HIGH.

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; P0MDIN Enums (Port 0 Input Mode @ 0xF1)

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P0MDIN\_B0\_\_BMASK EQU 001H ; Port 0 Bit 0 Input Mode

P0MDIN\_B0\_\_SHIFT EQU 000H ; Port 0 Bit 0 Input Mode

P0MDIN\_B0\_\_ANALOG EQU 000H ; P0.0 pin is configured for analog mode.

P0MDIN\_B0\_\_DIGITAL EQU 001H ; P0.0 pin is configured for digital mode.

P0MDIN\_B1\_\_BMASK EQU 002H ; Port 0 Bit 1 Input Mode

P0MDIN\_B1\_\_SHIFT EQU 001H ; Port 0 Bit 1 Input Mode

P0MDIN\_B1\_\_ANALOG EQU 000H ; P0.1 pin is configured for analog mode.

P0MDIN\_B1\_\_DIGITAL EQU 002H ; P0.1 pin is configured for digital mode.

P0MDIN\_B2\_\_BMASK EQU 004H ; Port 0 Bit 2 Input Mode

P0MDIN\_B2\_\_SHIFT EQU 002H ; Port 0 Bit 2 Input Mode

P0MDIN\_B2\_\_ANALOG EQU 000H ; P0.2 pin is configured for analog mode.

P0MDIN\_B2\_\_DIGITAL EQU 004H ; P0.2 pin is configured for digital mode.

P0MDIN\_B3\_\_BMASK EQU 008H ; Port 0 Bit 3 Input Mode

P0MDIN\_B3\_\_SHIFT EQU 003H ; Port 0 Bit 3 Input Mode

P0MDIN\_B3\_\_ANALOG EQU 000H ; P0.3 pin is configured for analog mode.

P0MDIN\_B3\_\_DIGITAL EQU 008H ; P0.3 pin is configured for digital mode.

P0MDIN\_B4\_\_BMASK EQU 010H ; Port 0 Bit 4 Input Mode

P0MDIN\_B4\_\_SHIFT EQU 004H ; Port 0 Bit 4 Input Mode

P0MDIN\_B4\_\_ANALOG EQU 000H ; P0.4 pin is configured for analog mode.

P0MDIN\_B4\_\_DIGITAL EQU 010H ; P0.4 pin is configured for digital mode.

P0MDIN\_B5\_\_BMASK EQU 020H ; Port 0 Bit 5 Input Mode

P0MDIN\_B5\_\_SHIFT EQU 005H ; Port 0 Bit 5 Input Mode

P0MDIN\_B5\_\_ANALOG EQU 000H ; P0.5 pin is configured for analog mode.

P0MDIN\_B5\_\_DIGITAL EQU 020H ; P0.5 pin is configured for digital mode.

P0MDIN\_B6\_\_BMASK EQU 040H ; Port 0 Bit 6 Input Mode

P0MDIN\_B6\_\_SHIFT EQU 006H ; Port 0 Bit 6 Input Mode

P0MDIN\_B6\_\_ANALOG EQU 000H ; P0.6 pin is configured for analog mode.

P0MDIN\_B6\_\_DIGITAL EQU 040H ; P0.6 pin is configured for digital mode.

P0MDIN\_B7\_\_BMASK EQU 080H ; Port 0 Bit 7 Input Mode

P0MDIN\_B7\_\_SHIFT EQU 007H ; Port 0 Bit 7 Input Mode

P0MDIN\_B7\_\_ANALOG EQU 000H ; P0.7 pin is configured for analog mode.

P0MDIN\_B7\_\_DIGITAL EQU 080H ; P0.7 pin is configured for digital mode.

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; P0MDOUT Enums (Port 0 Output Mode @ 0xA4)

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P0MDOUT\_B0\_\_BMASK EQU 001H ; Port 0 Bit 0 Output Mode

P0MDOUT\_B0\_\_SHIFT EQU 000H ; Port 0 Bit 0 Output Mode

P0MDOUT\_B0\_\_OPEN\_DRAIN EQU 000H ; P0.0 output is open-drain.

P0MDOUT\_B0\_\_PUSH\_PULL EQU 001H ; P0.0 output is push-pull.

P0MDOUT\_B1\_\_BMASK EQU 002H ; Port 0 Bit 1 Output Mode

P0MDOUT\_B1\_\_SHIFT EQU 001H ; Port 0 Bit 1 Output Mode

P0MDOUT\_B1\_\_OPEN\_DRAIN EQU 000H ; P0.1 output is open-drain.

P0MDOUT\_B1\_\_PUSH\_PULL EQU 002H ; P0.1 output is push-pull.

P0MDOUT\_B2\_\_BMASK EQU 004H ; Port 0 Bit 2 Output Mode

P0MDOUT\_B2\_\_SHIFT EQU 002H ; Port 0 Bit 2 Output Mode

P0MDOUT\_B2\_\_OPEN\_DRAIN EQU 000H ; P0.2 output is open-drain.

P0MDOUT\_B2\_\_PUSH\_PULL EQU 004H ; P0.2 output is push-pull.

P0MDOUT\_B3\_\_BMASK EQU 008H ; Port 0 Bit 3 Output Mode

P0MDOUT\_B3\_\_SHIFT EQU 003H ; Port 0 Bit 3 Output Mode

P0MDOUT\_B3\_\_OPEN\_DRAIN EQU 000H ; P0.3 output is open-drain.

P0MDOUT\_B3\_\_PUSH\_PULL EQU 008H ; P0.3 output is push-pull.

P0MDOUT\_B4\_\_BMASK EQU 010H ; Port 0 Bit 4 Output Mode

P0MDOUT\_B4\_\_SHIFT EQU 004H ; Port 0 Bit 4 Output Mode

P0MDOUT\_B4\_\_OPEN\_DRAIN EQU 000H ; P0.4 output is open-drain.

P0MDOUT\_B4\_\_PUSH\_PULL EQU 010H ; P0.4 output is push-pull.

P0MDOUT\_B5\_\_BMASK EQU 020H ; Port 0 Bit 5 Output Mode

P0MDOUT\_B5\_\_SHIFT EQU 005H ; Port 0 Bit 5 Output Mode

P0MDOUT\_B5\_\_OPEN\_DRAIN EQU 000H ; P0.5 output is open-drain.

P0MDOUT\_B5\_\_PUSH\_PULL EQU 020H ; P0.5 output is push-pull.

P0MDOUT\_B6\_\_BMASK EQU 040H ; Port 0 Bit 6 Output Mode

P0MDOUT\_B6\_\_SHIFT EQU 006H ; Port 0 Bit 6 Output Mode

P0MDOUT\_B6\_\_OPEN\_DRAIN EQU 000H ; P0.6 output is open-drain.

P0MDOUT\_B6\_\_PUSH\_PULL EQU 040H ; P0.6 output is push-pull.

P0MDOUT\_B7\_\_BMASK EQU 080H ; Port 0 Bit 7 Output Mode

P0MDOUT\_B7\_\_SHIFT EQU 007H ; Port 0 Bit 7 Output Mode

P0MDOUT\_B7\_\_OPEN\_DRAIN EQU 000H ; P0.7 output is open-drain.

P0MDOUT\_B7\_\_PUSH\_PULL EQU 080H ; P0.7 output is push-pull.

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; P0SKIP Enums (Port 0 Skip @ 0xD4)

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P0SKIP\_B0\_\_BMASK EQU 001H ; Port 0 Bit 0 Skip

P0SKIP\_B0\_\_SHIFT EQU 000H ; Port 0 Bit 0 Skip

P0SKIP\_B0\_\_NOT\_SKIPPED EQU 000H ; P0.0 pin is not skipped by the crossbar.

P0SKIP\_B0\_\_SKIPPED EQU 001H ; P0.0 pin is skipped by the crossbar.

P0SKIP\_B1\_\_BMASK EQU 002H ; Port 0 Bit 1 Skip

P0SKIP\_B1\_\_SHIFT EQU 001H ; Port 0 Bit 1 Skip

P0SKIP\_B1\_\_NOT\_SKIPPED EQU 000H ; P0.1 pin is not skipped by the crossbar.

P0SKIP\_B1\_\_SKIPPED EQU 002H ; P0.1 pin is skipped by the crossbar.

P0SKIP\_B2\_\_BMASK EQU 004H ; Port 0 Bit 2 Skip

P0SKIP\_B2\_\_SHIFT EQU 002H ; Port 0 Bit 2 Skip

P0SKIP\_B2\_\_NOT\_SKIPPED EQU 000H ; P0.2 pin is not skipped by the crossbar.

P0SKIP\_B2\_\_SKIPPED EQU 004H ; P0.2 pin is skipped by the crossbar.

P0SKIP\_B3\_\_BMASK EQU 008H ; Port 0 Bit 3 Skip

P0SKIP\_B3\_\_SHIFT EQU 003H ; Port 0 Bit 3 Skip

P0SKIP\_B3\_\_NOT\_SKIPPED EQU 000H ; P0.3 pin is not skipped by the crossbar.

P0SKIP\_B3\_\_SKIPPED EQU 008H ; P0.3 pin is skipped by the crossbar.

P0SKIP\_B4\_\_BMASK EQU 010H ; Port 0 Bit 4 Skip

P0SKIP\_B4\_\_SHIFT EQU 004H ; Port 0 Bit 4 Skip

P0SKIP\_B4\_\_NOT\_SKIPPED EQU 000H ; P0.4 pin is not skipped by the crossbar.

P0SKIP\_B4\_\_SKIPPED EQU 010H ; P0.4 pin is skipped by the crossbar.

P0SKIP\_B5\_\_BMASK EQU 020H ; Port 0 Bit 5 Skip

P0SKIP\_B5\_\_SHIFT EQU 005H ; Port 0 Bit 5 Skip

P0SKIP\_B5\_\_NOT\_SKIPPED EQU 000H ; P0.5 pin is not skipped by the crossbar.

P0SKIP\_B5\_\_SKIPPED EQU 020H ; P0.5 pin is skipped by the crossbar.

P0SKIP\_B6\_\_BMASK EQU 040H ; Port 0 Bit 6 Skip

P0SKIP\_B6\_\_SHIFT EQU 006H ; Port 0 Bit 6 Skip

P0SKIP\_B6\_\_NOT\_SKIPPED EQU 000H ; P0.6 pin is not skipped by the crossbar.

P0SKIP\_B6\_\_SKIPPED EQU 040H ; P0.6 pin is skipped by the crossbar.

P0SKIP\_B7\_\_BMASK EQU 080H ; Port 0 Bit 7 Skip

P0SKIP\_B7\_\_SHIFT EQU 007H ; Port 0 Bit 7 Skip

P0SKIP\_B7\_\_NOT\_SKIPPED EQU 000H ; P0.7 pin is not skipped by the crossbar.

P0SKIP\_B7\_\_SKIPPED EQU 080H ; P0.7 pin is skipped by the crossbar.

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; P1 Enums (Port 1 Pin Latch @ 0x90)

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P1\_B0\_\_BMASK EQU 001H ; Port 1 Bit 0 Latch

P1\_B0\_\_SHIFT EQU 000H ; Port 1 Bit 0 Latch

P1\_B0\_\_LOW EQU 000H ; P1.0 is low. Set P1.0 to drive low.

P1\_B0\_\_HIGH EQU 001H ; P1.0 is high. Set P1.0 to drive or float high.

P1\_B1\_\_BMASK EQU 002H ; Port 1 Bit 1 Latch

P1\_B1\_\_SHIFT EQU 001H ; Port 1 Bit 1 Latch

P1\_B1\_\_LOW EQU 000H ; P1.1 is low. Set P1.1 to drive low.

P1\_B1\_\_HIGH EQU 002H ; P1.1 is high. Set P1.1 to drive or float high.

P1\_B2\_\_BMASK EQU 004H ; Port 1 Bit 2 Latch

P1\_B2\_\_SHIFT EQU 002H ; Port 1 Bit 2 Latch

P1\_B2\_\_LOW EQU 000H ; P1.2 is low. Set P1.2 to drive low.

P1\_B2\_\_HIGH EQU 004H ; P1.2 is high. Set P1.2 to drive or float high.

P1\_B3\_\_BMASK EQU 008H ; Port 1 Bit 3 Latch

P1\_B3\_\_SHIFT EQU 003H ; Port 1 Bit 3 Latch

P1\_B3\_\_LOW EQU 000H ; P1.3 is low. Set P1.3 to drive low.

P1\_B3\_\_HIGH EQU 008H ; P1.3 is high. Set P1.3 to drive or float high.

P1\_B4\_\_BMASK EQU 010H ; Port 1 Bit 4 Latch

P1\_B4\_\_SHIFT EQU 004H ; Port 1 Bit 4 Latch

P1\_B4\_\_LOW EQU 000H ; P1.4 is low. Set P1.4 to drive low.

P1\_B4\_\_HIGH EQU 010H ; P1.4 is high. Set P1.4 to drive or float high.

P1\_B5\_\_BMASK EQU 020H ; Port 1 Bit 5 Latch

P1\_B5\_\_SHIFT EQU 005H ; Port 1 Bit 5 Latch

P1\_B5\_\_LOW EQU 000H ; P1.5 is low. Set P1.5 to drive low.

P1\_B5\_\_HIGH EQU 020H ; P1.5 is high. Set P1.5 to drive or float high.

P1\_B6\_\_BMASK EQU 040H ; Port 1 Bit 6 Latch

P1\_B6\_\_SHIFT EQU 006H ; Port 1 Bit 6 Latch

P1\_B6\_\_LOW EQU 000H ; P1.6 is low. Set P1.6 to drive low.

P1\_B6\_\_HIGH EQU 040H ; P1.6 is high. Set P1.6 to drive or float high.

P1\_B7\_\_BMASK EQU 080H ; Port 1 Bit 7 Latch

P1\_B7\_\_SHIFT EQU 007H ; Port 1 Bit 7 Latch

P1\_B7\_\_LOW EQU 000H ; P1.7 is low. Set P1.7 to drive low.

P1\_B7\_\_HIGH EQU 080H ; P1.7 is high. Set P1.7 to drive or float high.

;------------------------------------------------------------------------------

; P1MASK Enums (Port 1 Mask @ 0xEE)

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P1MASK\_B0\_\_BMASK EQU 001H ; Port 1 Bit 0 Mask Value

P1MASK\_B0\_\_SHIFT EQU 000H ; Port 1 Bit 0 Mask Value

P1MASK\_B0\_\_IGNORED EQU 000H ; P1.0 pin logic value is ignored and will not cause

; a port mismatch event.

P1MASK\_B0\_\_COMPARED EQU 001H ; P1.0 pin logic value is compared to P1MAT.0.

P1MASK\_B1\_\_BMASK EQU 002H ; Port 1 Bit 1 Mask Value

P1MASK\_B1\_\_SHIFT EQU 001H ; Port 1 Bit 1 Mask Value

P1MASK\_B1\_\_IGNORED EQU 000H ; P1.1 pin logic value is ignored and will not cause

; a port mismatch event.

P1MASK\_B1\_\_COMPARED EQU 002H ; P1.1 pin logic value is compared to P1MAT.1.

P1MASK\_B2\_\_BMASK EQU 004H ; Port 1 Bit 2 Mask Value

P1MASK\_B2\_\_SHIFT EQU 002H ; Port 1 Bit 2 Mask Value

P1MASK\_B2\_\_IGNORED EQU 000H ; P1.2 pin logic value is ignored and will not cause

; a port mismatch event.

P1MASK\_B2\_\_COMPARED EQU 004H ; P1.2 pin logic value is compared to P1MAT.2.

P1MASK\_B3\_\_BMASK EQU 008H ; Port 1 Bit 3 Mask Value

P1MASK\_B3\_\_SHIFT EQU 003H ; Port 1 Bit 3 Mask Value

P1MASK\_B3\_\_IGNORED EQU 000H ; P1.3 pin logic value is ignored and will not cause

; a port mismatch event.

P1MASK\_B3\_\_COMPARED EQU 008H ; P1.3 pin logic value is compared to P1MAT.3.

P1MASK\_B4\_\_BMASK EQU 010H ; Port 1 Bit 4 Mask Value

P1MASK\_B4\_\_SHIFT EQU 004H ; Port 1 Bit 4 Mask Value

P1MASK\_B4\_\_IGNORED EQU 000H ; P1.4 pin logic value is ignored and will not cause

; a port mismatch event.

P1MASK\_B4\_\_COMPARED EQU 010H ; P1.4 pin logic value is compared to P1MAT.4.

P1MASK\_B5\_\_BMASK EQU 020H ; Port 1 Bit 5 Mask Value

P1MASK\_B5\_\_SHIFT EQU 005H ; Port 1 Bit 5 Mask Value

P1MASK\_B5\_\_IGNORED EQU 000H ; P1.5 pin logic value is ignored and will not cause

; a port mismatch event.

P1MASK\_B5\_\_COMPARED EQU 020H ; P1.5 pin logic value is compared to P1MAT.5.

P1MASK\_B6\_\_BMASK EQU 040H ; Port 1 Bit 6 Mask Value

P1MASK\_B6\_\_SHIFT EQU 006H ; Port 1 Bit 6 Mask Value

P1MASK\_B6\_\_IGNORED EQU 000H ; P1.6 pin logic value is ignored and will not cause

; a port mismatch event.

P1MASK\_B6\_\_COMPARED EQU 040H ; P1.6 pin logic value is compared to P1MAT.6.

P1MASK\_B7\_\_BMASK EQU 080H ; Port 1 Bit 7 Mask Value

P1MASK\_B7\_\_SHIFT EQU 007H ; Port 1 Bit 7 Mask Value

P1MASK\_B7\_\_IGNORED EQU 000H ; P1.7 pin logic value is ignored and will not cause

; a port mismatch event.

P1MASK\_B7\_\_COMPARED EQU 080H ; P1.7 pin logic value is compared to P1MAT.7.

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; P1MAT Enums (Port 1 Match @ 0xED)

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P1MAT\_B0\_\_BMASK EQU 001H ; Port 1 Bit 0 Match Value

P1MAT\_B0\_\_SHIFT EQU 000H ; Port 1 Bit 0 Match Value

P1MAT\_B0\_\_LOW EQU 000H ; P1.0 pin logic value is compared with logic LOW.

P1MAT\_B0\_\_HIGH EQU 001H ; P1.0 pin logic value is compared with logic HIGH.

P1MAT\_B1\_\_BMASK EQU 002H ; Port 1 Bit 1 Match Value

P1MAT\_B1\_\_SHIFT EQU 001H ; Port 1 Bit 1 Match Value

P1MAT\_B1\_\_LOW EQU 000H ; P1.1 pin logic value is compared with logic LOW.

P1MAT\_B1\_\_HIGH EQU 002H ; P1.1 pin logic value is compared with logic HIGH.

P1MAT\_B2\_\_BMASK EQU 004H ; Port 1 Bit 2 Match Value

P1MAT\_B2\_\_SHIFT EQU 002H ; Port 1 Bit 2 Match Value

P1MAT\_B2\_\_LOW EQU 000H ; P1.2 pin logic value is compared with logic LOW.

P1MAT\_B2\_\_HIGH EQU 004H ; P1.2 pin logic value is compared with logic HIGH.

P1MAT\_B3\_\_BMASK EQU 008H ; Port 1 Bit 3 Match Value

P1MAT\_B3\_\_SHIFT EQU 003H ; Port 1 Bit 3 Match Value

P1MAT\_B3\_\_LOW EQU 000H ; P1.3 pin logic value is compared with logic LOW.

P1MAT\_B3\_\_HIGH EQU 008H ; P1.3 pin logic value is compared with logic HIGH.

P1MAT\_B4\_\_BMASK EQU 010H ; Port 1 Bit 4 Match Value

P1MAT\_B4\_\_SHIFT EQU 004H ; Port 1 Bit 4 Match Value

P1MAT\_B4\_\_LOW EQU 000H ; P1.4 pin logic value is compared with logic LOW.

P1MAT\_B4\_\_HIGH EQU 010H ; P1.4 pin logic value is compared with logic HIGH.

P1MAT\_B5\_\_BMASK EQU 020H ; Port 1 Bit 5 Match Value

P1MAT\_B5\_\_SHIFT EQU 005H ; Port 1 Bit 5 Match Value

P1MAT\_B5\_\_LOW EQU 000H ; P1.5 pin logic value is compared with logic LOW.

P1MAT\_B5\_\_HIGH EQU 020H ; P1.5 pin logic value is compared with logic HIGH.

P1MAT\_B6\_\_BMASK EQU 040H ; Port 1 Bit 6 Match Value

P1MAT\_B6\_\_SHIFT EQU 006H ; Port 1 Bit 6 Match Value

P1MAT\_B6\_\_LOW EQU 000H ; P1.6 pin logic value is compared with logic LOW.

P1MAT\_B6\_\_HIGH EQU 040H ; P1.6 pin logic value is compared with logic HIGH.

P1MAT\_B7\_\_BMASK EQU 080H ; Port 1 Bit 7 Match Value

P1MAT\_B7\_\_SHIFT EQU 007H ; Port 1 Bit 7 Match Value

P1MAT\_B7\_\_LOW EQU 000H ; P1.7 pin logic value is compared with logic LOW.

P1MAT\_B7\_\_HIGH EQU 080H ; P1.7 pin logic value is compared with logic HIGH.

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; P1MDIN Enums (Port 1 Input Mode @ 0xF2)

;------------------------------------------------------------------------------

P1MDIN\_B0\_\_BMASK EQU 001H ; Port 1 Bit 0 Input Mode

P1MDIN\_B0\_\_SHIFT EQU 000H ; Port 1 Bit 0 Input Mode

P1MDIN\_B0\_\_ANALOG EQU 000H ; P1.0 pin is configured for analog mode.

P1MDIN\_B0\_\_DIGITAL EQU 001H ; P1.0 pin is configured for digital mode.

P1MDIN\_B1\_\_BMASK EQU 002H ; Port 1 Bit 1 Input Mode

P1MDIN\_B1\_\_SHIFT EQU 001H ; Port 1 Bit 1 Input Mode

P1MDIN\_B1\_\_ANALOG EQU 000H ; P1.1 pin is configured for analog mode.

P1MDIN\_B1\_\_DIGITAL EQU 002H ; P1.1 pin is configured for digital mode.

P1MDIN\_B2\_\_BMASK EQU 004H ; Port 1 Bit 2 Input Mode

P1MDIN\_B2\_\_SHIFT EQU 002H ; Port 1 Bit 2 Input Mode

P1MDIN\_B2\_\_ANALOG EQU 000H ; P1.2 pin is configured for analog mode.

P1MDIN\_B2\_\_DIGITAL EQU 004H ; P1.2 pin is configured for digital mode.

P1MDIN\_B3\_\_BMASK EQU 008H ; Port 1 Bit 3 Input Mode

P1MDIN\_B3\_\_SHIFT EQU 003H ; Port 1 Bit 3 Input Mode

P1MDIN\_B3\_\_ANALOG EQU 000H ; P1.3 pin is configured for analog mode.

P1MDIN\_B3\_\_DIGITAL EQU 008H ; P1.3 pin is configured for digital mode.

P1MDIN\_B4\_\_BMASK EQU 010H ; Port 1 Bit 4 Input Mode

P1MDIN\_B4\_\_SHIFT EQU 004H ; Port 1 Bit 4 Input Mode

P1MDIN\_B4\_\_ANALOG EQU 000H ; P1.4 pin is configured for analog mode.

P1MDIN\_B4\_\_DIGITAL EQU 010H ; P1.4 pin is configured for digital mode.

P1MDIN\_B5\_\_BMASK EQU 020H ; Port 1 Bit 5 Input Mode

P1MDIN\_B5\_\_SHIFT EQU 005H ; Port 1 Bit 5 Input Mode

P1MDIN\_B5\_\_ANALOG EQU 000H ; P1.5 pin is configured for analog mode.

P1MDIN\_B5\_\_DIGITAL EQU 020H ; P1.5 pin is configured for digital mode.

P1MDIN\_B6\_\_BMASK EQU 040H ; Port 1 Bit 6 Input Mode

P1MDIN\_B6\_\_SHIFT EQU 006H ; Port 1 Bit 6 Input Mode

P1MDIN\_B6\_\_ANALOG EQU 000H ; P1.6 pin is configured for analog mode.

P1MDIN\_B6\_\_DIGITAL EQU 040H ; P1.6 pin is configured for digital mode.

P1MDIN\_B7\_\_BMASK EQU 080H ; Port 1 Bit 7 Input Mode

P1MDIN\_B7\_\_SHIFT EQU 007H ; Port 1 Bit 7 Input Mode

P1MDIN\_B7\_\_ANALOG EQU 000H ; P1.7 pin is configured for analog mode.

P1MDIN\_B7\_\_DIGITAL EQU 080H ; P1.7 pin is configured for digital mode.

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; P1MDOUT Enums (Port 1 Output Mode @ 0xA5)

;------------------------------------------------------------------------------

P1MDOUT\_B0\_\_BMASK EQU 001H ; Port 1 Bit 0 Output Mode

P1MDOUT\_B0\_\_SHIFT EQU 000H ; Port 1 Bit 0 Output Mode

P1MDOUT\_B0\_\_OPEN\_DRAIN EQU 000H ; P1.0 output is open-drain.

P1MDOUT\_B0\_\_PUSH\_PULL EQU 001H ; P1.0 output is push-pull.

P1MDOUT\_B1\_\_BMASK EQU 002H ; Port 1 Bit 1 Output Mode

P1MDOUT\_B1\_\_SHIFT EQU 001H ; Port 1 Bit 1 Output Mode

P1MDOUT\_B1\_\_OPEN\_DRAIN EQU 000H ; P1.1 output is open-drain.

P1MDOUT\_B1\_\_PUSH\_PULL EQU 002H ; P1.1 output is push-pull.

P1MDOUT\_B2\_\_BMASK EQU 004H ; Port 1 Bit 2 Output Mode

P1MDOUT\_B2\_\_SHIFT EQU 002H ; Port 1 Bit 2 Output Mode

P1MDOUT\_B2\_\_OPEN\_DRAIN EQU 000H ; P1.2 output is open-drain.

P1MDOUT\_B2\_\_PUSH\_PULL EQU 004H ; P1.2 output is push-pull.

P1MDOUT\_B3\_\_BMASK EQU 008H ; Port 1 Bit 3 Output Mode

P1MDOUT\_B3\_\_SHIFT EQU 003H ; Port 1 Bit 3 Output Mode

P1MDOUT\_B3\_\_OPEN\_DRAIN EQU 000H ; P1.3 output is open-drain.

P1MDOUT\_B3\_\_PUSH\_PULL EQU 008H ; P1.3 output is push-pull.

P1MDOUT\_B4\_\_BMASK EQU 010H ; Port 1 Bit 4 Output Mode

P1MDOUT\_B4\_\_SHIFT EQU 004H ; Port 1 Bit 4 Output Mode

P1MDOUT\_B4\_\_OPEN\_DRAIN EQU 000H ; P1.4 output is open-drain.

P1MDOUT\_B4\_\_PUSH\_PULL EQU 010H ; P1.4 output is push-pull.

P1MDOUT\_B5\_\_BMASK EQU 020H ; Port 1 Bit 5 Output Mode

P1MDOUT\_B5\_\_SHIFT EQU 005H ; Port 1 Bit 5 Output Mode

P1MDOUT\_B5\_\_OPEN\_DRAIN EQU 000H ; P1.5 output is open-drain.

P1MDOUT\_B5\_\_PUSH\_PULL EQU 020H ; P1.5 output is push-pull.

P1MDOUT\_B6\_\_BMASK EQU 040H ; Port 1 Bit 6 Output Mode

P1MDOUT\_B6\_\_SHIFT EQU 006H ; Port 1 Bit 6 Output Mode

P1MDOUT\_B6\_\_OPEN\_DRAIN EQU 000H ; P1.6 output is open-drain.

P1MDOUT\_B6\_\_PUSH\_PULL EQU 040H ; P1.6 output is push-pull.

P1MDOUT\_B7\_\_BMASK EQU 080H ; Port 1 Bit 7 Output Mode

P1MDOUT\_B7\_\_SHIFT EQU 007H ; Port 1 Bit 7 Output Mode

P1MDOUT\_B7\_\_OPEN\_DRAIN EQU 000H ; P1.7 output is open-drain.

P1MDOUT\_B7\_\_PUSH\_PULL EQU 080H ; P1.7 output is push-pull.

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; P1SKIP Enums (Port 1 Skip @ 0xD5)

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P1SKIP\_B0\_\_BMASK EQU 001H ; Port 1 Bit 0 Skip

P1SKIP\_B0\_\_SHIFT EQU 000H ; Port 1 Bit 0 Skip

P1SKIP\_B0\_\_NOT\_SKIPPED EQU 000H ; P1.0 pin is not skipped by the crossbar.

P1SKIP\_B0\_\_SKIPPED EQU 001H ; P1.0 pin is skipped by the crossbar.

P1SKIP\_B1\_\_BMASK EQU 002H ; Port 1 Bit 1 Skip

P1SKIP\_B1\_\_SHIFT EQU 001H ; Port 1 Bit 1 Skip

P1SKIP\_B1\_\_NOT\_SKIPPED EQU 000H ; P1.1 pin is not skipped by the crossbar.

P1SKIP\_B1\_\_SKIPPED EQU 002H ; P1.1 pin is skipped by the crossbar.

P1SKIP\_B2\_\_BMASK EQU 004H ; Port 1 Bit 2 Skip

P1SKIP\_B2\_\_SHIFT EQU 002H ; Port 1 Bit 2 Skip

P1SKIP\_B2\_\_NOT\_SKIPPED EQU 000H ; P1.2 pin is not skipped by the crossbar.

P1SKIP\_B2\_\_SKIPPED EQU 004H ; P1.2 pin is skipped by the crossbar.

P1SKIP\_B3\_\_BMASK EQU 008H ; Port 1 Bit 3 Skip

P1SKIP\_B3\_\_SHIFT EQU 003H ; Port 1 Bit 3 Skip

P1SKIP\_B3\_\_NOT\_SKIPPED EQU 000H ; P1.3 pin is not skipped by the crossbar.

P1SKIP\_B3\_\_SKIPPED EQU 008H ; P1.3 pin is skipped by the crossbar.

P1SKIP\_B4\_\_BMASK EQU 010H ; Port 1 Bit 4 Skip

P1SKIP\_B4\_\_SHIFT EQU 004H ; Port 1 Bit 4 Skip

P1SKIP\_B4\_\_NOT\_SKIPPED EQU 000H ; P1.4 pin is not skipped by the crossbar.

P1SKIP\_B4\_\_SKIPPED EQU 010H ; P1.4 pin is skipped by the crossbar.

P1SKIP\_B5\_\_BMASK EQU 020H ; Port 1 Bit 5 Skip

P1SKIP\_B5\_\_SHIFT EQU 005H ; Port 1 Bit 5 Skip

P1SKIP\_B5\_\_NOT\_SKIPPED EQU 000H ; P1.5 pin is not skipped by the crossbar.

P1SKIP\_B5\_\_SKIPPED EQU 020H ; P1.5 pin is skipped by the crossbar.

P1SKIP\_B6\_\_BMASK EQU 040H ; Port 1 Bit 6 Skip

P1SKIP\_B6\_\_SHIFT EQU 006H ; Port 1 Bit 6 Skip

P1SKIP\_B6\_\_NOT\_SKIPPED EQU 000H ; P1.6 pin is not skipped by the crossbar.

P1SKIP\_B6\_\_SKIPPED EQU 040H ; P1.6 pin is skipped by the crossbar.

P1SKIP\_B7\_\_BMASK EQU 080H ; Port 1 Bit 7 Skip

P1SKIP\_B7\_\_SHIFT EQU 007H ; Port 1 Bit 7 Skip

P1SKIP\_B7\_\_NOT\_SKIPPED EQU 000H ; P1.7 pin is not skipped by the crossbar.

P1SKIP\_B7\_\_SKIPPED EQU 080H ; P1.7 pin is skipped by the crossbar.

;------------------------------------------------------------------------------

; P2 Enums (Port 2 Pin Latch @ 0xA0)

;------------------------------------------------------------------------------

P2\_B0\_\_BMASK EQU 001H ; Port 2 Bit 0 Latch

P2\_B0\_\_SHIFT EQU 000H ; Port 2 Bit 0 Latch

P2\_B0\_\_LOW EQU 000H ; P2.0 is low. Set P2.0 to drive low.

P2\_B0\_\_HIGH EQU 001H ; P2.0 is high. Set P2.0 to drive or float high.

P2\_B1\_\_BMASK EQU 002H ; Port 2 Bit 1 Latch

P2\_B1\_\_SHIFT EQU 001H ; Port 2 Bit 1 Latch

P2\_B1\_\_LOW EQU 000H ; P2.1 is low. Set P2.1 to drive low.

P2\_B1\_\_HIGH EQU 002H ; P2.1 is high. Set P2.1 to drive or float high.

P2\_B2\_\_BMASK EQU 004H ; Port 2 Bit 2 Latch

P2\_B2\_\_SHIFT EQU 002H ; Port 2 Bit 2 Latch

P2\_B2\_\_LOW EQU 000H ; P2.2 is low. Set P2.2 to drive low.

P2\_B2\_\_HIGH EQU 004H ; P2.2 is high. Set P2.2 to drive or float high.

P2\_B3\_\_BMASK EQU 008H ; Port 2 Bit 3 Latch

P2\_B3\_\_SHIFT EQU 003H ; Port 2 Bit 3 Latch

P2\_B3\_\_LOW EQU 000H ; P2.3 is low. Set P2.3 to drive low.

P2\_B3\_\_HIGH EQU 008H ; P2.3 is high. Set P2.3 to drive or float high.

P2\_B4\_\_BMASK EQU 010H ; Port 2 Bit 4 Latch

P2\_B4\_\_SHIFT EQU 004H ; Port 2 Bit 4 Latch

P2\_B4\_\_LOW EQU 000H ; P2.4 is low. Set P2.4 to drive low.

P2\_B4\_\_HIGH EQU 010H ; P2.4 is high. Set P2.4 to drive or float high.

P2\_B5\_\_BMASK EQU 020H ; Port 2 Bit 5 Latch

P2\_B5\_\_SHIFT EQU 005H ; Port 2 Bit 5 Latch

P2\_B5\_\_LOW EQU 000H ; P2.5 is low. Set P2.5 to drive low.

P2\_B5\_\_HIGH EQU 020H ; P2.5 is high. Set P2.5 to drive or float high.

P2\_B6\_\_BMASK EQU 040H ; Port 2 Bit 6 Latch

P2\_B6\_\_SHIFT EQU 006H ; Port 2 Bit 6 Latch

P2\_B6\_\_LOW EQU 000H ; P2.6 is low. Set P2.6 to drive low.

P2\_B6\_\_HIGH EQU 040H ; P2.6 is high. Set P2.6 to drive or float high.

;------------------------------------------------------------------------------

; P2MASK Enums (Port 2 Mask @ 0xFC)

;------------------------------------------------------------------------------

P2MASK\_B0\_\_BMASK EQU 001H ; Port 2 Bit 0 Mask Value

P2MASK\_B0\_\_SHIFT EQU 000H ; Port 2 Bit 0 Mask Value

P2MASK\_B0\_\_IGNORED EQU 000H ; P2.0 pin logic value is ignored and will not cause

; a port mismatch event.

P2MASK\_B0\_\_COMPARED EQU 001H ; P2.0 pin logic value is compared to P2MAT.0.

P2MASK\_B1\_\_BMASK EQU 002H ; Port 2 Bit 1 Mask Value

P2MASK\_B1\_\_SHIFT EQU 001H ; Port 2 Bit 1 Mask Value

P2MASK\_B1\_\_IGNORED EQU 000H ; P2.1 pin logic value is ignored and will not cause

; a port mismatch event.

P2MASK\_B1\_\_COMPARED EQU 002H ; P2.1 pin logic value is compared to P2MAT.1.

P2MASK\_B2\_\_BMASK EQU 004H ; Port 2 Bit 2 Mask Value

P2MASK\_B2\_\_SHIFT EQU 002H ; Port 2 Bit 2 Mask Value

P2MASK\_B2\_\_IGNORED EQU 000H ; P2.2 pin logic value is ignored and will not cause

; a port mismatch event.

P2MASK\_B2\_\_COMPARED EQU 004H ; P2.2 pin logic value is compared to P2MAT.2.

P2MASK\_B3\_\_BMASK EQU 008H ; Port 2 Bit 3 Mask Value

P2MASK\_B3\_\_SHIFT EQU 003H ; Port 2 Bit 3 Mask Value

P2MASK\_B3\_\_IGNORED EQU 000H ; P2.3 pin logic value is ignored and will not cause

; a port mismatch event.

P2MASK\_B3\_\_COMPARED EQU 008H ; P2.3 pin logic value is compared to P2MAT.3.

P2MASK\_B4\_\_BMASK EQU 010H ; Port 2 Bit 4 Mask Value

P2MASK\_B4\_\_SHIFT EQU 004H ; Port 2 Bit 4 Mask Value

P2MASK\_B4\_\_IGNORED EQU 000H ; P2.4 pin logic value is ignored and will not cause

; a port mismatch event.

P2MASK\_B4\_\_COMPARED EQU 010H ; P2.4 pin logic value is compared to P2MAT.4.

P2MASK\_B5\_\_BMASK EQU 020H ; Port 2 Bit 5 Mask Value

P2MASK\_B5\_\_SHIFT EQU 005H ; Port 2 Bit 5 Mask Value

P2MASK\_B5\_\_IGNORED EQU 000H ; P2.5 pin logic value is ignored and will not cause

; a port mismatch event.

P2MASK\_B5\_\_COMPARED EQU 020H ; P2.5 pin logic value is compared to P2MAT.5.

P2MASK\_B6\_\_BMASK EQU 040H ; Port 2 Bit 6 Mask Value

P2MASK\_B6\_\_SHIFT EQU 006H ; Port 2 Bit 6 Mask Value

P2MASK\_B6\_\_IGNORED EQU 000H ; P2.6 pin logic value is ignored and will not cause

; a port mismatch event.

P2MASK\_B6\_\_COMPARED EQU 040H ; P2.6 pin logic value is compared to P2MAT.6.

;------------------------------------------------------------------------------

; P2MAT Enums (Port 2 Match @ 0xFB)

;------------------------------------------------------------------------------

P2MAT\_B0\_\_BMASK EQU 001H ; Port 2 Bit 0 Match Value

P2MAT\_B0\_\_SHIFT EQU 000H ; Port 2 Bit 0 Match Value

P2MAT\_B0\_\_LOW EQU 000H ; P2.0 pin logic value is compared with logic LOW.

P2MAT\_B0\_\_HIGH EQU 001H ; P2.0 pin logic value is compared with logic HIGH.

P2MAT\_B1\_\_BMASK EQU 002H ; Port 2 Bit 1 Match Value

P2MAT\_B1\_\_SHIFT EQU 001H ; Port 2 Bit 1 Match Value

P2MAT\_B1\_\_LOW EQU 000H ; P2.1 pin logic value is compared with logic LOW.

P2MAT\_B1\_\_HIGH EQU 002H ; P2.1 pin logic value is compared with logic HIGH.

P2MAT\_B2\_\_BMASK EQU 004H ; Port 2 Bit 2 Match Value

P2MAT\_B2\_\_SHIFT EQU 002H ; Port 2 Bit 2 Match Value

P2MAT\_B2\_\_LOW EQU 000H ; P2.2 pin logic value is compared with logic LOW.

P2MAT\_B2\_\_HIGH EQU 004H ; P2.2 pin logic value is compared with logic HIGH.

P2MAT\_B3\_\_BMASK EQU 008H ; Port 2 Bit 3 Match Value

P2MAT\_B3\_\_SHIFT EQU 003H ; Port 2 Bit 3 Match Value

P2MAT\_B3\_\_LOW EQU 000H ; P2.3 pin logic value is compared with logic LOW.

P2MAT\_B3\_\_HIGH EQU 008H ; P2.3 pin logic value is compared with logic HIGH.

P2MAT\_B4\_\_BMASK EQU 010H ; Port 2 Bit 4 Match Value

P2MAT\_B4\_\_SHIFT EQU 004H ; Port 2 Bit 4 Match Value

P2MAT\_B4\_\_LOW EQU 000H ; P2.4 pin logic value is compared with logic LOW.

P2MAT\_B4\_\_HIGH EQU 010H ; P2.4 pin logic value is compared with logic HIGH.

P2MAT\_B5\_\_BMASK EQU 020H ; Port 2 Bit 5 Match Value

P2MAT\_B5\_\_SHIFT EQU 005H ; Port 2 Bit 5 Match Value

P2MAT\_B5\_\_LOW EQU 000H ; P2.5 pin logic value is compared with logic LOW.

P2MAT\_B5\_\_HIGH EQU 020H ; P2.5 pin logic value is compared with logic HIGH.

P2MAT\_B6\_\_BMASK EQU 040H ; Port 2 Bit 6 Match Value

P2MAT\_B6\_\_SHIFT EQU 006H ; Port 2 Bit 6 Match Value

P2MAT\_B6\_\_LOW EQU 000H ; P2.6 pin logic value is compared with logic LOW.

P2MAT\_B6\_\_HIGH EQU 040H ; P2.6 pin logic value is compared with logic HIGH.

;------------------------------------------------------------------------------

; P2MDIN Enums (Port 2 Input Mode @ 0xF3)

;------------------------------------------------------------------------------

P2MDIN\_B0\_\_BMASK EQU 001H ; Port 2 Bit 0 Input Mode

P2MDIN\_B0\_\_SHIFT EQU 000H ; Port 2 Bit 0 Input Mode

P2MDIN\_B0\_\_ANALOG EQU 000H ; P2.0 pin is configured for analog mode.

P2MDIN\_B0\_\_DIGITAL EQU 001H ; P2.0 pin is configured for digital mode.

P2MDIN\_B1\_\_BMASK EQU 002H ; Port 2 Bit 1 Input Mode

P2MDIN\_B1\_\_SHIFT EQU 001H ; Port 2 Bit 1 Input Mode

P2MDIN\_B1\_\_ANALOG EQU 000H ; P2.1 pin is configured for analog mode.

P2MDIN\_B1\_\_DIGITAL EQU 002H ; P2.1 pin is configured for digital mode.

P2MDIN\_B2\_\_BMASK EQU 004H ; Port 2 Bit 2 Input Mode

P2MDIN\_B2\_\_SHIFT EQU 002H ; Port 2 Bit 2 Input Mode

P2MDIN\_B2\_\_ANALOG EQU 000H ; P2.2 pin is configured for analog mode.

P2MDIN\_B2\_\_DIGITAL EQU 004H ; P2.2 pin is configured for digital mode.

P2MDIN\_B3\_\_BMASK EQU 008H ; Port 2 Bit 3 Input Mode

P2MDIN\_B3\_\_SHIFT EQU 003H ; Port 2 Bit 3 Input Mode

P2MDIN\_B3\_\_ANALOG EQU 000H ; P2.3 pin is configured for analog mode.

P2MDIN\_B3\_\_DIGITAL EQU 008H ; P2.3 pin is configured for digital mode.

P2MDIN\_B4\_\_BMASK EQU 010H ; Port 2 Bit 4 Input Mode

P2MDIN\_B4\_\_SHIFT EQU 004H ; Port 2 Bit 4 Input Mode

P2MDIN\_B4\_\_ANALOG EQU 000H ; P2.4 pin is configured for analog mode.

P2MDIN\_B4\_\_DIGITAL EQU 010H ; P2.4 pin is configured for digital mode.

P2MDIN\_B5\_\_BMASK EQU 020H ; Port 2 Bit 5 Input Mode

P2MDIN\_B5\_\_SHIFT EQU 005H ; Port 2 Bit 5 Input Mode

P2MDIN\_B5\_\_ANALOG EQU 000H ; P2.5 pin is configured for analog mode.

P2MDIN\_B5\_\_DIGITAL EQU 020H ; P2.5 pin is configured for digital mode.

P2MDIN\_B6\_\_BMASK EQU 040H ; Port 2 Bit 6 Input Mode

P2MDIN\_B6\_\_SHIFT EQU 006H ; Port 2 Bit 6 Input Mode

P2MDIN\_B6\_\_ANALOG EQU 000H ; P2.6 pin is configured for analog mode.

P2MDIN\_B6\_\_DIGITAL EQU 040H ; P2.6 pin is configured for digital mode.

;------------------------------------------------------------------------------

; P2MDOUT Enums (Port 2 Output Mode @ 0xA6)

;------------------------------------------------------------------------------

P2MDOUT\_B0\_\_BMASK EQU 001H ; Port 2 Bit 0 Output Mode

P2MDOUT\_B0\_\_SHIFT EQU 000H ; Port 2 Bit 0 Output Mode

P2MDOUT\_B0\_\_OPEN\_DRAIN EQU 000H ; P2.0 output is open-drain.

P2MDOUT\_B0\_\_PUSH\_PULL EQU 001H ; P2.0 output is push-pull.

P2MDOUT\_B1\_\_BMASK EQU 002H ; Port 2 Bit 1 Output Mode

P2MDOUT\_B1\_\_SHIFT EQU 001H ; Port 2 Bit 1 Output Mode

P2MDOUT\_B1\_\_OPEN\_DRAIN EQU 000H ; P2.1 output is open-drain.

P2MDOUT\_B1\_\_PUSH\_PULL EQU 002H ; P2.1 output is push-pull.

P2MDOUT\_B2\_\_BMASK EQU 004H ; Port 2 Bit 2 Output Mode

P2MDOUT\_B2\_\_SHIFT EQU 002H ; Port 2 Bit 2 Output Mode

P2MDOUT\_B2\_\_OPEN\_DRAIN EQU 000H ; P2.2 output is open-drain.

P2MDOUT\_B2\_\_PUSH\_PULL EQU 004H ; P2.2 output is push-pull.

P2MDOUT\_B3\_\_BMASK EQU 008H ; Port 2 Bit 3 Output Mode

P2MDOUT\_B3\_\_SHIFT EQU 003H ; Port 2 Bit 3 Output Mode

P2MDOUT\_B3\_\_OPEN\_DRAIN EQU 000H ; P2.3 output is open-drain.

P2MDOUT\_B3\_\_PUSH\_PULL EQU 008H ; P2.3 output is push-pull.

P2MDOUT\_B4\_\_BMASK EQU 010H ; Port 2 Bit 4 Output Mode

P2MDOUT\_B4\_\_SHIFT EQU 004H ; Port 2 Bit 4 Output Mode

P2MDOUT\_B4\_\_OPEN\_DRAIN EQU 000H ; P2.4 output is open-drain.

P2MDOUT\_B4\_\_PUSH\_PULL EQU 010H ; P2.4 output is push-pull.

P2MDOUT\_B5\_\_BMASK EQU 020H ; Port 2 Bit 5 Output Mode

P2MDOUT\_B5\_\_SHIFT EQU 005H ; Port 2 Bit 5 Output Mode

P2MDOUT\_B5\_\_OPEN\_DRAIN EQU 000H ; P2.5 output is open-drain.

P2MDOUT\_B5\_\_PUSH\_PULL EQU 020H ; P2.5 output is push-pull.

P2MDOUT\_B6\_\_BMASK EQU 040H ; Port 2 Bit 6 Output Mode

P2MDOUT\_B6\_\_SHIFT EQU 006H ; Port 2 Bit 6 Output Mode

P2MDOUT\_B6\_\_OPEN\_DRAIN EQU 000H ; P2.6 output is open-drain.

P2MDOUT\_B6\_\_PUSH\_PULL EQU 040H ; P2.6 output is push-pull.

;------------------------------------------------------------------------------

; P2SKIP Enums (Port 2 Skip @ 0xCC)

;------------------------------------------------------------------------------

P2SKIP\_B0\_\_BMASK EQU 001H ; Port 2 Bit 0 Skip

P2SKIP\_B0\_\_SHIFT EQU 000H ; Port 2 Bit 0 Skip

P2SKIP\_B0\_\_NOT\_SKIPPED EQU 000H ; P2.0 pin is not skipped by the crossbar.

P2SKIP\_B0\_\_SKIPPED EQU 001H ; P2.0 pin is skipped by the crossbar.

P2SKIP\_B1\_\_BMASK EQU 002H ; Port 2 Bit 1 Skip

P2SKIP\_B1\_\_SHIFT EQU 001H ; Port 2 Bit 1 Skip

P2SKIP\_B1\_\_NOT\_SKIPPED EQU 000H ; P2.1 pin is not skipped by the crossbar.

P2SKIP\_B1\_\_SKIPPED EQU 002H ; P2.1 pin is skipped by the crossbar.

P2SKIP\_B2\_\_BMASK EQU 004H ; Port 2 Bit 2 Skip

P2SKIP\_B2\_\_SHIFT EQU 002H ; Port 2 Bit 2 Skip

P2SKIP\_B2\_\_NOT\_SKIPPED EQU 000H ; P2.2 pin is not skipped by the crossbar.

P2SKIP\_B2\_\_SKIPPED EQU 004H ; P2.2 pin is skipped by the crossbar.

P2SKIP\_B3\_\_BMASK EQU 008H ; Port 2 Bit 3 Skip

P2SKIP\_B3\_\_SHIFT EQU 003H ; Port 2 Bit 3 Skip

P2SKIP\_B3\_\_NOT\_SKIPPED EQU 000H ; P2.3 pin is not skipped by the crossbar.

P2SKIP\_B3\_\_SKIPPED EQU 008H ; P2.3 pin is skipped by the crossbar.

;------------------------------------------------------------------------------

; P3 Enums (Port 3 Pin Latch @ 0xB0)

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P3\_B0\_\_BMASK EQU 001H ; Port 3 Bit 0 Latch

P3\_B0\_\_SHIFT EQU 000H ; Port 3 Bit 0 Latch

P3\_B0\_\_LOW EQU 000H ; P3.0 is low. Set P3.0 to drive low.

P3\_B0\_\_HIGH EQU 001H ; P3.0 is high. Set P3.0 to drive or float high.

P3\_B1\_\_BMASK EQU 002H ; Port 3 Bit 1 Latch

P3\_B1\_\_SHIFT EQU 001H ; Port 3 Bit 1 Latch

P3\_B1\_\_LOW EQU 000H ; P3.1 is low. Set P3.1 to drive low.

P3\_B1\_\_HIGH EQU 002H ; P3.1 is high. Set P3.1 to drive or float high.

P3\_B2\_\_BMASK EQU 004H ; Port 3 Bit 2 Latch

P3\_B2\_\_SHIFT EQU 002H ; Port 3 Bit 2 Latch

P3\_B2\_\_LOW EQU 000H ; P3.2 is low. Set P3.2 to drive low.

P3\_B2\_\_HIGH EQU 004H ; P3.2 is high. Set P3.2 to drive or float high.

P3\_B3\_\_BMASK EQU 008H ; Port 3 Bit 3 Latch

P3\_B3\_\_SHIFT EQU 003H ; Port 3 Bit 3 Latch

P3\_B3\_\_LOW EQU 000H ; P3.3 is low. Set P3.3 to drive low.

P3\_B3\_\_HIGH EQU 008H ; P3.3 is high. Set P3.3 to drive or float high.

P3\_B4\_\_BMASK EQU 010H ; Port 3 Bit 4 Latch

P3\_B4\_\_SHIFT EQU 004H ; Port 3 Bit 4 Latch

P3\_B4\_\_LOW EQU 000H ; P3.4 is low. Set P3.4 to drive low.

P3\_B4\_\_HIGH EQU 010H ; P3.4 is high. Set P3.4 to drive or float high.

P3\_B7\_\_BMASK EQU 080H ; Port 3 Bit 7 Latch

P3\_B7\_\_SHIFT EQU 007H ; Port 3 Bit 7 Latch

P3\_B7\_\_LOW EQU 000H ; P3.7 is low. Set P3.7 to drive low.

P3\_B7\_\_HIGH EQU 080H ; P3.7 is high. Set P3.7 to drive or float high.

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; P3MDIN Enums (Port 3 Input Mode @ 0xF4)

;------------------------------------------------------------------------------

P3MDIN\_B0\_\_BMASK EQU 001H ; Port 3 Bit 0 Input Mode

P3MDIN\_B0\_\_SHIFT EQU 000H ; Port 3 Bit 0 Input Mode

P3MDIN\_B0\_\_ANALOG EQU 000H ; P3.0 pin is configured for analog mode.

P3MDIN\_B0\_\_DIGITAL EQU 001H ; P3.0 pin is configured for digital mode.

P3MDIN\_B1\_\_BMASK EQU 002H ; Port 3 Bit 1 Input Mode

P3MDIN\_B1\_\_SHIFT EQU 001H ; Port 3 Bit 1 Input Mode

P3MDIN\_B1\_\_ANALOG EQU 000H ; P3.1 pin is configured for analog mode.

P3MDIN\_B1\_\_DIGITAL EQU 002H ; P3.1 pin is configured for digital mode.

P3MDIN\_B2\_\_BMASK EQU 004H ; Port 3 Bit 2 Input Mode

P3MDIN\_B2\_\_SHIFT EQU 002H ; Port 3 Bit 2 Input Mode

P3MDIN\_B2\_\_ANALOG EQU 000H ; P3.2 pin is configured for analog mode.

P3MDIN\_B2\_\_DIGITAL EQU 004H ; P3.2 pin is configured for digital mode.

P3MDIN\_B3\_\_BMASK EQU 008H ; Port 3 Bit 3 Input Mode

P3MDIN\_B3\_\_SHIFT EQU 003H ; Port 3 Bit 3 Input Mode

P3MDIN\_B3\_\_ANALOG EQU 000H ; P3.3 pin is configured for analog mode.

P3MDIN\_B3\_\_DIGITAL EQU 008H ; P3.3 pin is configured for digital mode.

P3MDIN\_B4\_\_BMASK EQU 010H ; Port 3 Bit 4 Input Mode

P3MDIN\_B4\_\_SHIFT EQU 004H ; Port 3 Bit 4 Input Mode

P3MDIN\_B4\_\_ANALOG EQU 000H ; P3.4 pin is configured for analog mode.

P3MDIN\_B4\_\_DIGITAL EQU 010H ; P3.4 pin is configured for digital mode.

P3MDIN\_B7\_\_BMASK EQU 080H ; Port 3 Bit 7 Input Mode

P3MDIN\_B7\_\_SHIFT EQU 007H ; Port 3 Bit 7 Input Mode

P3MDIN\_B7\_\_ANALOG EQU 000H ; P3.7 pin is configured for analog mode.

P3MDIN\_B7\_\_DIGITAL EQU 080H ; P3.7 pin is configured for digital mode.

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; P3MDOUT Enums (Port 3 Output Mode @ 0x9C)

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P3MDOUT\_B0\_\_BMASK EQU 001H ; Port 3 Bit 0 Output Mode

P3MDOUT\_B0\_\_SHIFT EQU 000H ; Port 3 Bit 0 Output Mode

P3MDOUT\_B0\_\_OPEN\_DRAIN EQU 000H ; P3.0 output is open-drain.

P3MDOUT\_B0\_\_PUSH\_PULL EQU 001H ; P3.0 output is push-pull.

P3MDOUT\_B1\_\_BMASK EQU 002H ; Port 3 Bit 1 Output Mode

P3MDOUT\_B1\_\_SHIFT EQU 001H ; Port 3 Bit 1 Output Mode

P3MDOUT\_B1\_\_OPEN\_DRAIN EQU 000H ; P3.1 output is open-drain.

P3MDOUT\_B1\_\_PUSH\_PULL EQU 002H ; P3.1 output is push-pull.

P3MDOUT\_B2\_\_BMASK EQU 004H ; Port 3 Bit 2 Output Mode

P3MDOUT\_B2\_\_SHIFT EQU 002H ; Port 3 Bit 2 Output Mode

P3MDOUT\_B2\_\_OPEN\_DRAIN EQU 000H ; P3.2 output is open-drain.

P3MDOUT\_B2\_\_PUSH\_PULL EQU 004H ; P3.2 output is push-pull.

P3MDOUT\_B3\_\_BMASK EQU 008H ; Port 3 Bit 3 Output Mode

P3MDOUT\_B3\_\_SHIFT EQU 003H ; Port 3 Bit 3 Output Mode

P3MDOUT\_B3\_\_OPEN\_DRAIN EQU 000H ; P3.3 output is open-drain.

P3MDOUT\_B3\_\_PUSH\_PULL EQU 008H ; P3.3 output is push-pull.

P3MDOUT\_B4\_\_BMASK EQU 010H ; Port 3 Bit 4 Output Mode

P3MDOUT\_B4\_\_SHIFT EQU 004H ; Port 3 Bit 4 Output Mode

P3MDOUT\_B4\_\_OPEN\_DRAIN EQU 000H ; P3.4 output is open-drain.

P3MDOUT\_B4\_\_PUSH\_PULL EQU 010H ; P3.4 output is push-pull.

P3MDOUT\_B7\_\_BMASK EQU 080H ; Port 3 Bit 7 Output Mode

P3MDOUT\_B7\_\_SHIFT EQU 007H ; Port 3 Bit 7 Output Mode

P3MDOUT\_B7\_\_OPEN\_DRAIN EQU 000H ; P3.7 output is open-drain.

P3MDOUT\_B7\_\_PUSH\_PULL EQU 080H ; P3.7 output is push-pull.

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; RSTSRC Enums (Reset Source @ 0xEF)

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RSTSRC\_PINRSF\_\_BMASK EQU 001H ; HW Pin Reset Flag

RSTSRC\_PINRSF\_\_SHIFT EQU 000H ; HW Pin Reset Flag

RSTSRC\_PINRSF\_\_NOT\_SET EQU 000H ; The RSTb pin did not cause the last reset.

RSTSRC\_PINRSF\_\_SET EQU 001H ; The RSTb pin caused the last reset.

RSTSRC\_PORSF\_\_BMASK EQU 002H ; Power-On / Supply Monitor Reset Flag, and Supply Monitor Reset Enable

RSTSRC\_PORSF\_\_SHIFT EQU 001H ; Power-On / Supply Monitor Reset Flag, and Supply Monitor Reset Enable

RSTSRC\_PORSF\_\_NOT\_SET EQU 000H ; A power-on or supply monitor reset did not occur.

RSTSRC\_PORSF\_\_SET EQU 002H ; A power-on or supply monitor reset occurred.

RSTSRC\_MCDRSF\_\_BMASK EQU 004H ; Missing Clock Detector Enable and Flag

RSTSRC\_MCDRSF\_\_SHIFT EQU 002H ; Missing Clock Detector Enable and Flag

RSTSRC\_MCDRSF\_\_NOT\_SET EQU 000H ; A missing clock detector reset did not occur.

RSTSRC\_MCDRSF\_\_SET EQU 004H ; A missing clock detector reset occurred.

RSTSRC\_WDTRSF\_\_BMASK EQU 008H ; Watchdog Timer Reset Flag

RSTSRC\_WDTRSF\_\_SHIFT EQU 003H ; Watchdog Timer Reset Flag

RSTSRC\_WDTRSF\_\_NOT\_SET EQU 000H ; A watchdog timer overflow reset did not occur.

RSTSRC\_WDTRSF\_\_SET EQU 008H ; A watchdog timer overflow reset occurred.

RSTSRC\_SWRSF\_\_BMASK EQU 010H ; Software Reset Force and Flag

RSTSRC\_SWRSF\_\_SHIFT EQU 004H ; Software Reset Force and Flag

RSTSRC\_SWRSF\_\_NOT\_SET EQU 000H ; A software reset did not occur.

RSTSRC\_SWRSF\_\_SET EQU 010H ; A software reset occurred.

RSTSRC\_C0RSEF\_\_BMASK EQU 020H ; Comparator0 Reset Enable and Flag

RSTSRC\_C0RSEF\_\_SHIFT EQU 005H ; Comparator0 Reset Enable and Flag

RSTSRC\_C0RSEF\_\_NOT\_SET EQU 000H ; A Comparator 0 reset did not occur.

RSTSRC\_C0RSEF\_\_SET EQU 020H ; A Comparator 0 reset occurred.

RSTSRC\_FERROR\_\_BMASK EQU 040H ; Flash Error Reset Flag

RSTSRC\_FERROR\_\_SHIFT EQU 006H ; Flash Error Reset Flag

RSTSRC\_FERROR\_\_NOT\_SET EQU 000H ; A flash error reset did not occur.

RSTSRC\_FERROR\_\_SET EQU 040H ; A flash error reset occurred.

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; SFRPAGE Enums (SFR Page @ 0xA7)

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SFRPAGE\_SFRPAGE\_\_FMASK EQU 0FFH ; SFR Page

SFRPAGE\_SFRPAGE\_\_SHIFT EQU 000H ; SFR Page

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; SFRPGCN Enums (SFR Page Control @ 0xBC)

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SFRPGCN\_SFRPGEN\_\_BMASK EQU 001H ; SFR Automatic Page Control Enable

SFRPGCN\_SFRPGEN\_\_SHIFT EQU 000H ; SFR Automatic Page Control Enable

SFRPGCN\_SFRPGEN\_\_DISABLED EQU 000H ; Disable automatic SFR paging.

SFRPGCN\_SFRPGEN\_\_ENABLED EQU 001H ; Enable automatic SFR paging.

SFRPGCN\_SFRPGIDX\_\_FMASK EQU 070H ; SFR Page Stack Index

SFRPGCN\_SFRPGIDX\_\_SHIFT EQU 004H ; SFR Page Stack Index

SFRPGCN\_SFRPGIDX\_\_FIRST\_BYTE EQU 000H ; SFRSTACK contains the value of SFRPAGE, the

; first/top byte of the SFR page stack.

SFRPGCN\_SFRPGIDX\_\_SECOND\_BYTE EQU 010H ; SFRSTACK contains the value of the second byte of

; the SFR page stack.

SFRPGCN\_SFRPGIDX\_\_THIRD\_BYTE EQU 020H ; SFRSTACK contains the value of the third byte of

; the SFR page stack.

SFRPGCN\_SFRPGIDX\_\_FOURTH\_BYTE EQU 030H ; SFRSTACK contains the value of the fourth byte of

; the SFR page stack.

SFRPGCN\_SFRPGIDX\_\_FIFTH\_BYTE EQU 040H ; SFRSTACK contains the value of the fifth byte of

; the SFR page stack.

;------------------------------------------------------------------------------

; SFRSTACK Enums (SFR Page Stack @ 0xD7)

;------------------------------------------------------------------------------

SFRSTACK\_SFRSTACK\_\_FMASK EQU 0FFH ; SFR Page Stack

SFRSTACK\_SFRSTACK\_\_SHIFT EQU 000H ; SFR Page Stack

;------------------------------------------------------------------------------

; SMB0ADM Enums (SMBus 0 Slave Address Mask @ 0xD6)

;------------------------------------------------------------------------------

SMB0ADM\_EHACK\_\_BMASK EQU 001H ; Hardware Acknowledge Enable

SMB0ADM\_EHACK\_\_SHIFT EQU 000H ; Hardware Acknowledge Enable

SMB0ADM\_EHACK\_\_ADR\_ACK\_MANUAL EQU 000H ; Firmware must manually acknowledge all incoming

; address and data bytes.

SMB0ADM\_EHACK\_\_ADR\_ACK\_AUTOMATIC EQU 001H ; Automatic slave address recognition and hardware

; acknowledge is enabled.

SMB0ADM\_SLVM\_\_FMASK EQU 0FEH ; SMBus Slave Address Mask

SMB0ADM\_SLVM\_\_SHIFT EQU 001H ; SMBus Slave Address Mask

;------------------------------------------------------------------------------

; SMB0ADR Enums (SMBus 0 Slave Address @ 0xD7)

;------------------------------------------------------------------------------

SMB0ADR\_GC\_\_BMASK EQU 001H ; General Call Address Enable

SMB0ADR\_GC\_\_SHIFT EQU 000H ; General Call Address Enable

SMB0ADR\_GC\_\_IGNORED EQU 000H ; General Call Address is ignored.

SMB0ADR\_GC\_\_RECOGNIZED EQU 001H ; General Call Address is recognized.

SMB0ADR\_SLV\_\_FMASK EQU 0FEH ; SMBus Hardware Slave Address

SMB0ADR\_SLV\_\_SHIFT EQU 001H ; SMBus Hardware Slave Address

;------------------------------------------------------------------------------

; SMB0CF Enums (SMBus 0 Configuration @ 0xC1)

;------------------------------------------------------------------------------

SMB0CF\_SMBCS\_\_FMASK EQU 003H ; SMBus Clock Source Selection

SMB0CF\_SMBCS\_\_SHIFT EQU 000H ; SMBus Clock Source Selection

SMB0CF\_SMBCS\_\_TIMER0 EQU 000H ; Timer 0 Overflow.

SMB0CF\_SMBCS\_\_TIMER1 EQU 001H ; Timer 1 Overflow.

SMB0CF\_SMBCS\_\_TIMER2\_HIGH EQU 002H ; Timer 2 High Byte Overflow.

SMB0CF\_SMBCS\_\_TIMER2\_LOW EQU 003H ; Timer 2 Low Byte Overflow.

SMB0CF\_SMBFTE\_\_BMASK EQU 004H ; SMBus Free Timeout Detection Enable

SMB0CF\_SMBFTE\_\_SHIFT EQU 002H ; SMBus Free Timeout Detection Enable

SMB0CF\_SMBFTE\_\_FREE\_TO\_DISABLED EQU 000H ; Disable bus free timeouts.

SMB0CF\_SMBFTE\_\_FREE\_TO\_ENABLED EQU 004H ; Enable bus free timeouts. The bus the bus will be

; considered free if SCL and SDA remain high for

; more than 10 SMBus clock source periods.

SMB0CF\_SMBTOE\_\_BMASK EQU 008H ; SMBus SCL Timeout Detection Enable

SMB0CF\_SMBTOE\_\_SHIFT EQU 003H ; SMBus SCL Timeout Detection Enable

SMB0CF\_SMBTOE\_\_SCL\_TO\_DISABLED EQU 000H ; Disable SCL low timeouts.

SMB0CF\_SMBTOE\_\_SCL\_TO\_ENABLED EQU 008H ; Enable SCL low timeouts if Timer 3 RLFSEL is set

; appropriately.

SMB0CF\_EXTHOLD\_\_BMASK EQU 010H ; SMBus Setup and Hold Time Extension Enable

SMB0CF\_EXTHOLD\_\_SHIFT EQU 004H ; SMBus Setup and Hold Time Extension Enable

SMB0CF\_EXTHOLD\_\_DISABLED EQU 000H ; Disable SDA extended setup and hold times.

SMB0CF\_EXTHOLD\_\_ENABLED EQU 010H ; Enable SDA extended setup and hold times.

SMB0CF\_BUSY\_\_BMASK EQU 020H ; SMBus Busy Indicator

SMB0CF\_BUSY\_\_SHIFT EQU 005H ; SMBus Busy Indicator

SMB0CF\_BUSY\_\_NOT\_SET EQU 000H ; The bus is not busy.

SMB0CF\_BUSY\_\_SET EQU 020H ; The bus is busy and a transfer is currently in

; progress.

SMB0CF\_INH\_\_BMASK EQU 040H ; SMBus Slave Inhibit

SMB0CF\_INH\_\_SHIFT EQU 006H ; SMBus Slave Inhibit

SMB0CF\_INH\_\_SLAVE\_ENABLED EQU 000H ; Slave states are enabled.

SMB0CF\_INH\_\_SLAVE\_DISABLED EQU 040H ; Slave states are inhibited.

SMB0CF\_ENSMB\_\_BMASK EQU 080H ; SMBus Enable

SMB0CF\_ENSMB\_\_SHIFT EQU 007H ; SMBus Enable

SMB0CF\_ENSMB\_\_DISABLED EQU 000H ; Disable the SMBus module.

SMB0CF\_ENSMB\_\_ENABLED EQU 080H ; Enable the SMBus module.

;------------------------------------------------------------------------------

; SMB0CN0 Enums (SMBus 0 Control @ 0xC0)

;------------------------------------------------------------------------------

SMB0CN0\_SI\_\_BMASK EQU 001H ; SMBus Interrupt Flag

SMB0CN0\_SI\_\_SHIFT EQU 000H ; SMBus Interrupt Flag

SMB0CN0\_SI\_\_NOT\_SET EQU 000H ;

SMB0CN0\_SI\_\_SET EQU 001H ;

SMB0CN0\_ACK\_\_BMASK EQU 002H ; SMBus Acknowledge

SMB0CN0\_ACK\_\_SHIFT EQU 001H ; SMBus Acknowledge

SMB0CN0\_ACK\_\_NOT\_SET EQU 000H ; Generate a NACK, or the response was a NACK.

SMB0CN0\_ACK\_\_SET EQU 002H ; Generate an ACK, or the response was an ACK.

SMB0CN0\_ARBLOST\_\_BMASK EQU 004H ; SMBus Arbitration Lost Indicator

SMB0CN0\_ARBLOST\_\_SHIFT EQU 002H ; SMBus Arbitration Lost Indicator

SMB0CN0\_ARBLOST\_\_NOT\_SET EQU 000H ; No arbitration error.

SMB0CN0\_ARBLOST\_\_ERROR EQU 004H ; Arbitration error occurred.

SMB0CN0\_ACKRQ\_\_BMASK EQU 008H ; SMBus Acknowledge Request

SMB0CN0\_ACKRQ\_\_SHIFT EQU 003H ; SMBus Acknowledge Request

SMB0CN0\_ACKRQ\_\_NOT\_SET EQU 000H ; No ACK requested.

SMB0CN0\_ACKRQ\_\_REQUESTED EQU 008H ; ACK requested.

SMB0CN0\_STO\_\_BMASK EQU 010H ; SMBus Stop Flag

SMB0CN0\_STO\_\_SHIFT EQU 004H ; SMBus Stop Flag

SMB0CN0\_STO\_\_NOT\_SET EQU 000H ; A STOP is not pending.

SMB0CN0\_STO\_\_SET EQU 010H ; Generate a STOP or a STOP is currently pending.

SMB0CN0\_STA\_\_BMASK EQU 020H ; SMBus Start Flag

SMB0CN0\_STA\_\_SHIFT EQU 005H ; SMBus Start Flag

SMB0CN0\_STA\_\_NOT\_SET EQU 000H ; A START was not detected.

SMB0CN0\_STA\_\_SET EQU 020H ; Generate a START, repeated START, or a START is

; currently pending.

SMB0CN0\_TXMODE\_\_BMASK EQU 040H ; SMBus Transmit Mode Indicator

SMB0CN0\_TXMODE\_\_SHIFT EQU 006H ; SMBus Transmit Mode Indicator

SMB0CN0\_TXMODE\_\_RECEIVER EQU 000H ; SMBus in Receiver Mode.

SMB0CN0\_TXMODE\_\_TRANSMITTER EQU 040H ; SMBus in Transmitter Mode.

SMB0CN0\_MASTER\_\_BMASK EQU 080H ; SMBus Master/Slave Indicator

SMB0CN0\_MASTER\_\_SHIFT EQU 007H ; SMBus Master/Slave Indicator

SMB0CN0\_MASTER\_\_SLAVE EQU 000H ; SMBus operating in slave mode.

SMB0CN0\_MASTER\_\_MASTER EQU 080H ; SMBus operating in master mode.

;------------------------------------------------------------------------------

; SMB0DAT Enums (SMBus 0 Data @ 0xC2)

;------------------------------------------------------------------------------

SMB0DAT\_SMB0DAT\_\_FMASK EQU 0FFH ; SMBus 0 Data

SMB0DAT\_SMB0DAT\_\_SHIFT EQU 000H ; SMBus 0 Data

;------------------------------------------------------------------------------

; SMB0FCN0 Enums (SMBus 0 FIFO Control 0 @ 0xC3)

;------------------------------------------------------------------------------

SMB0FCN0\_RXTH\_\_FMASK EQU 003H ; RX FIFO Threshold

SMB0FCN0\_RXTH\_\_SHIFT EQU 000H ; RX FIFO Threshold

SMB0FCN0\_RXTH\_\_ZERO EQU 000H ; RFRQ will be set anytime new data arrives in the

; RX FIFO (when the RX FIFO is not empty).

SMB0FCN0\_RFLSH\_\_BMASK EQU 004H ; RX FIFO Flush

SMB0FCN0\_RFLSH\_\_SHIFT EQU 002H ; RX FIFO Flush

SMB0FCN0\_RFLSH\_\_FLUSH EQU 004H ; Initiate an RX FIFO flush.

SMB0FCN0\_RFRQE\_\_BMASK EQU 008H ; Read Request Interrupt Enable

SMB0FCN0\_RFRQE\_\_SHIFT EQU 003H ; Read Request Interrupt Enable

SMB0FCN0\_RFRQE\_\_DISABLED EQU 000H ; SMBus 0 interrupts will not be generated when RFRQ

; is set.

SMB0FCN0\_RFRQE\_\_ENABLED EQU 008H ; SMBus 0 interrupts will be generated if RFRQ is

; set.

SMB0FCN0\_TXTH\_\_FMASK EQU 030H ; TX FIFO Threshold

SMB0FCN0\_TXTH\_\_SHIFT EQU 004H ; TX FIFO Threshold

SMB0FCN0\_TXTH\_\_ZERO EQU 000H ; TFRQ will be set when the TX FIFO is empty.

SMB0FCN0\_TFLSH\_\_BMASK EQU 040H ; TX FIFO Flush

SMB0FCN0\_TFLSH\_\_SHIFT EQU 006H ; TX FIFO Flush

SMB0FCN0\_TFLSH\_\_FLUSH EQU 040H ; Initiate a TX FIFO flush.

SMB0FCN0\_TFRQE\_\_BMASK EQU 080H ; Write Request Interrupt Enable

SMB0FCN0\_TFRQE\_\_SHIFT EQU 007H ; Write Request Interrupt Enable

SMB0FCN0\_TFRQE\_\_DISABLED EQU 000H ; SMBus 0 interrupts will not be generated when TFRQ

; is set.

SMB0FCN0\_TFRQE\_\_ENABLED EQU 080H ; SMBus 0 interrupts will be generated if TFRQ is

; set.

;------------------------------------------------------------------------------

; SMB0FCN1 Enums (SMBus 0 FIFO Control 1 @ 0xC4)

;------------------------------------------------------------------------------

SMB0FCN1\_RXE\_\_BMASK EQU 004H ; RX FIFO Empty

SMB0FCN1\_RXE\_\_SHIFT EQU 002H ; RX FIFO Empty

SMB0FCN1\_RXE\_\_NOT\_EMPTY EQU 000H ; The RX FIFO contains data.

SMB0FCN1\_RXE\_\_EMPTY EQU 004H ; The RX FIFO is empty.

SMB0FCN1\_RFRQ\_\_BMASK EQU 008H ; Receive FIFO Request

SMB0FCN1\_RFRQ\_\_SHIFT EQU 003H ; Receive FIFO Request

SMB0FCN1\_RFRQ\_\_NOT\_SET EQU 000H ; The number of bytes in the RX FIFO is less than or

; equal to RXTH.

SMB0FCN1\_RFRQ\_\_SET EQU 008H ; The number of bytes in the RX FIFO is greater than

; RXTH.

SMB0FCN1\_TXNF\_\_BMASK EQU 040H ; TX FIFO Not Full

SMB0FCN1\_TXNF\_\_SHIFT EQU 006H ; TX FIFO Not Full

SMB0FCN1\_TXNF\_\_FULL EQU 000H ; The TX FIFO is full.

SMB0FCN1\_TXNF\_\_NOT\_FULL EQU 040H ; The TX FIFO has room for more data.

SMB0FCN1\_TFRQ\_\_BMASK EQU 080H ; Transmit FIFO Request

SMB0FCN1\_TFRQ\_\_SHIFT EQU 007H ; Transmit FIFO Request

SMB0FCN1\_TFRQ\_\_NOT\_SET EQU 000H ; The number of bytes in the TX FIFO is greater than

; TXTH.

SMB0FCN1\_TFRQ\_\_SET EQU 080H ; The number of bytes in the TX FIFO is less than or

; equal to TXTH.

;------------------------------------------------------------------------------

; SMB0FCT Enums (SMBus 0 FIFO Count @ 0xEF)

;------------------------------------------------------------------------------

SMB0FCT\_RXCNT\_\_BMASK EQU 001H ; RX FIFO Count

SMB0FCT\_RXCNT\_\_SHIFT EQU 000H ; RX FIFO Count

SMB0FCT\_TXCNT\_\_BMASK EQU 010H ; TX FIFO Count

SMB0FCT\_TXCNT\_\_SHIFT EQU 004H ; TX FIFO Count

;------------------------------------------------------------------------------

; SMB0RXLN Enums (SMBus 0 Receive Length Counter @ 0xC5)

;------------------------------------------------------------------------------

SMB0RXLN\_RXLN\_\_FMASK EQU 0FFH ; SMBus Receive Length Counter

SMB0RXLN\_RXLN\_\_SHIFT EQU 000H ; SMBus Receive Length Counter

;------------------------------------------------------------------------------

; SMB0TC Enums (SMBus 0 Timing and Pin Control @ 0xAC)

;------------------------------------------------------------------------------

SMB0TC\_SDD\_\_FMASK EQU 003H ; SMBus Start Detection Window

SMB0TC\_SDD\_\_SHIFT EQU 000H ; SMBus Start Detection Window

SMB0TC\_SDD\_\_NONE EQU 000H ; No additional hold time window (0-1 SYSCLK).

SMB0TC\_SDD\_\_ADD\_2\_SYSCLKS EQU 001H ; Increase hold time window to 2-3 SYSCLKs.

SMB0TC\_SDD\_\_ADD\_4\_SYSCLKS EQU 002H ; Increase hold time window to 4-5 SYSCLKs.

SMB0TC\_SDD\_\_ADD\_8\_SYSCLKS EQU 003H ; Increase hold time window to 8-9 SYSCLKs.

SMB0TC\_DLYEXT\_\_BMASK EQU 010H ; Setup and Hold Delay Extension

SMB0TC\_DLYEXT\_\_SHIFT EQU 004H ; Setup and Hold Delay Extension

SMB0TC\_DLYEXT\_\_STANDARD EQU 000H ; SDA setup time is 11 SYSCLKs and SDA hold time is

; 12 SYSCLKs.

SMB0TC\_DLYEXT\_\_EXTENDED EQU 010H ; SDA setup time is 31 SYSCLKs and SDA hold time is

; 31 SYSCLKs.

SMB0TC\_SWAP\_\_BMASK EQU 080H ; SMBus Swap Pins

SMB0TC\_SWAP\_\_SHIFT EQU 007H ; SMBus Swap Pins

SMB0TC\_SWAP\_\_SDA\_LOW\_PIN EQU 000H ; SDA is mapped to the lower-numbered port pin, and

; SCL is mapped to the higher-numbered port pin.

SMB0TC\_SWAP\_\_SDA\_HIGH\_PIN EQU 080H ; SCL is mapped to the lower-numbered port pin, and

; SDA is mapped to the higher-numbered port pin.

;------------------------------------------------------------------------------

; SPI0CFG Enums (SPI0 Configuration @ 0xA1)

;------------------------------------------------------------------------------

SPI0CFG\_RXE\_\_BMASK EQU 001H ; RX FIFO Empty

SPI0CFG\_RXE\_\_SHIFT EQU 000H ; RX FIFO Empty

SPI0CFG\_RXE\_\_NOT\_EMPTY EQU 000H ; The RX FIFO contains data.

SPI0CFG\_RXE\_\_EMPTY EQU 001H ; The RX FIFO is empty.

SPI0CFG\_SRMT\_\_BMASK EQU 002H ; Shift Register Empty

SPI0CFG\_SRMT\_\_SHIFT EQU 001H ; Shift Register Empty

SPI0CFG\_SRMT\_\_NOT\_SET EQU 000H ; The shift register is not empty.

SPI0CFG\_SRMT\_\_SET EQU 002H ; The shift register is empty.

SPI0CFG\_NSSIN\_\_BMASK EQU 004H ; NSS Instantaneous Pin Input

SPI0CFG\_NSSIN\_\_SHIFT EQU 002H ; NSS Instantaneous Pin Input

SPI0CFG\_NSSIN\_\_LOW EQU 000H ; The NSS pin is low.

SPI0CFG\_NSSIN\_\_HIGH EQU 004H ; The NSS pin is high.

SPI0CFG\_SLVSEL\_\_BMASK EQU 008H ; Slave Selected Flag

SPI0CFG\_SLVSEL\_\_SHIFT EQU 003H ; Slave Selected Flag

SPI0CFG\_SLVSEL\_\_NOT\_SELECTED EQU 000H ; The Slave is not selected (NSS is high).

SPI0CFG\_SLVSEL\_\_SELECTED EQU 008H ; The Slave is selected (NSS is low).

SPI0CFG\_CKPOL\_\_BMASK EQU 010H ; SPI0 Clock Polarity

SPI0CFG\_CKPOL\_\_SHIFT EQU 004H ; SPI0 Clock Polarity

SPI0CFG\_CKPOL\_\_IDLE\_LOW EQU 000H ; SCK line low in idle state.

SPI0CFG\_CKPOL\_\_IDLE\_HIGH EQU 010H ; SCK line high in idle state.

SPI0CFG\_CKPHA\_\_BMASK EQU 020H ; SPI0 Clock Phase

SPI0CFG\_CKPHA\_\_SHIFT EQU 005H ; SPI0 Clock Phase

SPI0CFG\_CKPHA\_\_DATA\_CENTERED\_FIRST EQU 000H ; Data centered on first edge of SCK period.

SPI0CFG\_CKPHA\_\_DATA\_CENTERED\_SECOND EQU 020H ; Data centered on second edge of SCK period.

SPI0CFG\_MSTEN\_\_BMASK EQU 040H ; Master Mode Enable

SPI0CFG\_MSTEN\_\_SHIFT EQU 006H ; Master Mode Enable

SPI0CFG\_MSTEN\_\_MASTER\_DISABLED EQU 000H ; Disable master mode. Operate in slave mode.

SPI0CFG\_MSTEN\_\_MASTER\_ENABLED EQU 040H ; Enable master mode. Operate as a master.

SPI0CFG\_SPIBSY\_\_BMASK EQU 080H ; SPI Busy

SPI0CFG\_SPIBSY\_\_SHIFT EQU 007H ; SPI Busy

SPI0CFG\_SPIBSY\_\_NOT\_SET EQU 000H ; A SPI transfer is not in progress.

SPI0CFG\_SPIBSY\_\_SET EQU 080H ; A SPI transfer is in progress.

;------------------------------------------------------------------------------

; SPI0CKR Enums (SPI0 Clock Rate @ 0xA2)

;------------------------------------------------------------------------------

SPI0CKR\_SPI0CKR\_\_FMASK EQU 0FFH ; SPI0 Clock Rate

SPI0CKR\_SPI0CKR\_\_SHIFT EQU 000H ; SPI0 Clock Rate

;------------------------------------------------------------------------------

; SPI0CN0 Enums (SPI0 Control @ 0xF8)

;------------------------------------------------------------------------------

SPI0CN0\_SPIEN\_\_BMASK EQU 001H ; SPI0 Enable

SPI0CN0\_SPIEN\_\_SHIFT EQU 000H ; SPI0 Enable

SPI0CN0\_SPIEN\_\_DISABLED EQU 000H ; Disable the SPI module.

SPI0CN0\_SPIEN\_\_ENABLED EQU 001H ; Enable the SPI module.

SPI0CN0\_TXNF\_\_BMASK EQU 002H ; TX FIFO Not Full

SPI0CN0\_TXNF\_\_SHIFT EQU 001H ; TX FIFO Not Full

SPI0CN0\_TXNF\_\_FULL EQU 000H ; The TX FIFO is full.

SPI0CN0\_TXNF\_\_NOT\_FULL EQU 002H ; The TX FIFO has room for more data.

SPI0CN0\_NSSMD\_\_FMASK EQU 00CH ; Slave Select Mode

SPI0CN0\_NSSMD\_\_SHIFT EQU 002H ; Slave Select Mode

SPI0CN0\_NSSMD\_\_3\_WIRE EQU 000H ; 3-Wire Slave or 3-Wire Master Mode. NSS signal is

; not routed to a port pin.

SPI0CN0\_NSSMD\_\_4\_WIRE\_SLAVE EQU 004H ; 4-Wire Slave or Multi-Master Mode. NSS is an input

; to the device.

SPI0CN0\_NSSMD\_\_4\_WIRE\_MASTER\_NSS\_LOW EQU 008H ; 4-Wire Single-Master Mode. NSS is an output and

; logic low.

SPI0CN0\_NSSMD\_\_4\_WIRE\_MASTER\_NSS\_HIGH EQU 00CH ; 4-Wire Single-Master Mode. NSS is an output and

; logic high.

SPI0CN0\_RXOVRN\_\_BMASK EQU 010H ; Receive Overrun Flag

SPI0CN0\_RXOVRN\_\_SHIFT EQU 004H ; Receive Overrun Flag

SPI0CN0\_RXOVRN\_\_NOT\_SET EQU 000H ; A receive overrun did not occur.

SPI0CN0\_RXOVRN\_\_SET EQU 010H ; A receive overrun occurred.

SPI0CN0\_MODF\_\_BMASK EQU 020H ; Mode Fault Flag

SPI0CN0\_MODF\_\_SHIFT EQU 005H ; Mode Fault Flag

SPI0CN0\_MODF\_\_NOT\_SET EQU 000H ; A master collision did not occur.

SPI0CN0\_MODF\_\_SET EQU 020H ; A master collision occurred.

SPI0CN0\_WCOL\_\_BMASK EQU 040H ; Write Collision Flag

SPI0CN0\_WCOL\_\_SHIFT EQU 006H ; Write Collision Flag

SPI0CN0\_WCOL\_\_NOT\_SET EQU 000H ; A write collision did not occur.

SPI0CN0\_WCOL\_\_SET EQU 040H ; A write collision occurred.

SPI0CN0\_SPIF\_\_BMASK EQU 080H ; SPI0 Interrupt Flag

SPI0CN0\_SPIF\_\_SHIFT EQU 007H ; SPI0 Interrupt Flag

SPI0CN0\_SPIF\_\_NOT\_SET EQU 000H ; A data transfer has not completed since the last

; time SPIF was cleared.

SPI0CN0\_SPIF\_\_SET EQU 080H ; A data transfer completed.

;------------------------------------------------------------------------------

; SPI0DAT Enums (SPI0 Data @ 0xA3)

;------------------------------------------------------------------------------

SPI0DAT\_SPI0DAT\_\_FMASK EQU 0FFH ; SPI0 Transmit and Receive Data

SPI0DAT\_SPI0DAT\_\_SHIFT EQU 000H ; SPI0 Transmit and Receive Data

;------------------------------------------------------------------------------

; SPI0FCN0 Enums (SPI0 FIFO Control 0 @ 0x9A)

;------------------------------------------------------------------------------

SPI0FCN0\_RXTH\_\_FMASK EQU 003H ; RX FIFO Threshold

SPI0FCN0\_RXTH\_\_SHIFT EQU 000H ; RX FIFO Threshold

SPI0FCN0\_RXTH\_\_ZERO EQU 000H ; RFRQ will be set anytime new data arrives in the

; RX FIFO (when the RX FIFO is not empty).

SPI0FCN0\_RXTH\_\_ONE EQU 001H ; RFRQ will be set if the RX FIFO contains more than

; one byte.

SPI0FCN0\_RFLSH\_\_BMASK EQU 004H ; RX FIFO Flush

SPI0FCN0\_RFLSH\_\_SHIFT EQU 002H ; RX FIFO Flush

SPI0FCN0\_RFLSH\_\_FLUSH EQU 004H ; Initiate an RX FIFO flush.

SPI0FCN0\_RFRQE\_\_BMASK EQU 008H ; Read Request Interrupt Enable

SPI0FCN0\_RFRQE\_\_SHIFT EQU 003H ; Read Request Interrupt Enable

SPI0FCN0\_RFRQE\_\_DISABLED EQU 000H ; SPI0 interrupts will not be generated when RFRQ is

; set.

SPI0FCN0\_RFRQE\_\_ENABLED EQU 008H ; SPI0 interrupts will be generated if RFRQ is set.

SPI0FCN0\_TXTH\_\_FMASK EQU 030H ; TX FIFO Threshold

SPI0FCN0\_TXTH\_\_SHIFT EQU 004H ; TX FIFO Threshold

SPI0FCN0\_TXTH\_\_ZERO EQU 000H ; TFRQ will be set when the TX FIFO is empty.

SPI0FCN0\_TXTH\_\_ONE EQU 010H ; TFRQ will be set when the TX FIFO contains one or

; fewer bytes.

SPI0FCN0\_TFLSH\_\_BMASK EQU 040H ; TX FIFO Flush

SPI0FCN0\_TFLSH\_\_SHIFT EQU 006H ; TX FIFO Flush

SPI0FCN0\_TFLSH\_\_FLUSH EQU 040H ; Initiate a TX FIFO flush.

SPI0FCN0\_TFRQE\_\_BMASK EQU 080H ; Write Request Interrupt Enable

SPI0FCN0\_TFRQE\_\_SHIFT EQU 007H ; Write Request Interrupt Enable

SPI0FCN0\_TFRQE\_\_DISABLED EQU 000H ; SPI0 interrupts will not be generated when TFRQ is

; set.

SPI0FCN0\_TFRQE\_\_ENABLED EQU 080H ; SPI0 interrupts will be generated if TFRQ is set.

;------------------------------------------------------------------------------

; SPI0FCN1 Enums (SPI0 FIFO Control 1 @ 0x9B)

;------------------------------------------------------------------------------

SPI0FCN1\_RXFIFOE\_\_BMASK EQU 001H ; Receive FIFO Enable

SPI0FCN1\_RXFIFOE\_\_SHIFT EQU 000H ; Receive FIFO Enable

SPI0FCN1\_RXFIFOE\_\_DISABLED EQU 000H ; Received bytes will be discarded.

SPI0FCN1\_RXFIFOE\_\_ENABLED EQU 001H ; Received bytes will be placed in the RX FIFO.

SPI0FCN1\_RXTOE\_\_BMASK EQU 002H ; Receive Timeout Enable

SPI0FCN1\_RXTOE\_\_SHIFT EQU 001H ; Receive Timeout Enable

SPI0FCN1\_RXTOE\_\_DISABLED EQU 000H ; Lingering bytes in the RX FIFO will not generate

; an interrupt.

SPI0FCN1\_RXTOE\_\_ENABLED EQU 002H ; Lingering bytes in the RX FIFO will generate an

; interrupt after timeout.

SPI0FCN1\_RFRQ\_\_BMASK EQU 008H ; Receive FIFO Request

SPI0FCN1\_RFRQ\_\_SHIFT EQU 003H ; Receive FIFO Request

SPI0FCN1\_RFRQ\_\_NOT\_SET EQU 000H ; The number of bytes in the RX FIFO is less than or

; equal to RXTH.

SPI0FCN1\_RFRQ\_\_SET EQU 008H ; The number of bytes in the RX FIFO is greater than

; RXTH.

SPI0FCN1\_SPIFEN\_\_BMASK EQU 010H ; SPIF Interrupt Enable

SPI0FCN1\_SPIFEN\_\_SHIFT EQU 004H ; SPIF Interrupt Enable

SPI0FCN1\_SPIFEN\_\_DISABLED EQU 000H ; SPI0 interrupts will not be generated when SPIF is

; set.

SPI0FCN1\_SPIFEN\_\_ENABLED EQU 010H ; SPI0 interrupts will be generated if SPIF is set.

SPI0FCN1\_TXHOLD\_\_BMASK EQU 020H ; Transmit Hold

SPI0FCN1\_TXHOLD\_\_SHIFT EQU 005H ; Transmit Hold

SPI0FCN1\_TXHOLD\_\_CONTINUE EQU 000H ; The UART will continue to transmit any available

; data in the TX FIFO.

SPI0FCN1\_TXHOLD\_\_HOLD EQU 020H ; The UART will not transmit any new data from the

; TX FIFO.

SPI0FCN1\_THPOL\_\_BMASK EQU 040H ; Transmit Hold Polarity

SPI0FCN1\_THPOL\_\_SHIFT EQU 006H ; Transmit Hold Polarity

SPI0FCN1\_THPOL\_\_HOLD\_0 EQU 000H ; Data output will be held at logic low when TXHOLD

; is set.

SPI0FCN1\_THPOL\_\_HOLD\_1 EQU 040H ; Data output will be held at logic high when TXHOLD

; is set.

SPI0FCN1\_TFRQ\_\_BMASK EQU 080H ; Transmit FIFO Request

SPI0FCN1\_TFRQ\_\_SHIFT EQU 007H ; Transmit FIFO Request

SPI0FCN1\_TFRQ\_\_NOT\_SET EQU 000H ; The number of bytes in the TX FIFO is greater than

; TXTH.

SPI0FCN1\_TFRQ\_\_SET EQU 080H ; The number of bytes in the TX FIFO is less than or

; equal to TXTH.

;------------------------------------------------------------------------------

; SPI0FCT Enums (SPI0 FIFO Count @ 0xF7)

;------------------------------------------------------------------------------

SPI0FCT\_RXCNT\_\_FMASK EQU 007H ; RX FIFO Count

SPI0FCT\_RXCNT\_\_SHIFT EQU 000H ; RX FIFO Count

SPI0FCT\_TXCNT\_\_FMASK EQU 070H ; TX FIFO Count

SPI0FCT\_TXCNT\_\_SHIFT EQU 004H ; TX FIFO Count

;------------------------------------------------------------------------------

; SPI0PCF Enums (SPI0 Pin Configuration @ 0xDF)

;------------------------------------------------------------------------------

SPI0PCF\_SISEL\_\_BMASK EQU 001H ; Slave Data Input Select

SPI0PCF\_SISEL\_\_SHIFT EQU 000H ; Slave Data Input Select

SPI0PCF\_SISEL\_\_CROSSBAR EQU 000H ; MOSI (slave mode data input) is connected to the

; pin assigned by the crossbar.

SPI0PCF\_SISEL\_\_CLU3 EQU 001H ; MOSI (slave mode data input) is connected to the

; CLU3 output.

SPI0PCF\_MISEL\_\_BMASK EQU 002H ; Master Data Input Select

SPI0PCF\_MISEL\_\_SHIFT EQU 001H ; Master Data Input Select

SPI0PCF\_MISEL\_\_CROSSBAR EQU 000H ; MISO (master mode data input) is connected to the

; pin assigned by the crossbar.

SPI0PCF\_MISEL\_\_CLU2 EQU 002H ; MISO (master mode data input) is connected to the

; CLU2 output.

SPI0PCF\_SCKSEL\_\_BMASK EQU 004H ; Slave Clock Input Select

SPI0PCF\_SCKSEL\_\_SHIFT EQU 002H ; Slave Clock Input Select

SPI0PCF\_SCKSEL\_\_CROSSBAR EQU 000H ; SCK (slave mode clock input) is connected to the

; pin assigned by the crossbar.

SPI0PCF\_SCKSEL\_\_CLU1 EQU 004H ; SCK (slave mode clock input) is connected to the

; CLU1 output.

;------------------------------------------------------------------------------

; TH0 Enums (Timer 0 High Byte @ 0x8C)

;------------------------------------------------------------------------------

TH0\_TH0\_\_FMASK EQU 0FFH ; Timer 0 High Byte

TH0\_TH0\_\_SHIFT EQU 000H ; Timer 0 High Byte

;------------------------------------------------------------------------------

; TH1 Enums (Timer 1 High Byte @ 0x8D)

;------------------------------------------------------------------------------

TH1\_TH1\_\_FMASK EQU 0FFH ; Timer 1 High Byte

TH1\_TH1\_\_SHIFT EQU 000H ; Timer 1 High Byte

;------------------------------------------------------------------------------

; TL0 Enums (Timer 0 Low Byte @ 0x8A)

;------------------------------------------------------------------------------

TL0\_TL0\_\_FMASK EQU 0FFH ; Timer 0 Low Byte

TL0\_TL0\_\_SHIFT EQU 000H ; Timer 0 Low Byte

;------------------------------------------------------------------------------

; TL1 Enums (Timer 1 Low Byte @ 0x8B)

;------------------------------------------------------------------------------

TL1\_TL1\_\_FMASK EQU 0FFH ; Timer 1 Low Byte

TL1\_TL1\_\_SHIFT EQU 000H ; Timer 1 Low Byte

;------------------------------------------------------------------------------

; TMR2CN0 Enums (Timer 2 Control 0 @ 0xC8)

;------------------------------------------------------------------------------

TMR2CN0\_T2XCLK\_\_FMASK EQU 003H ; Timer 2 External Clock Select

TMR2CN0\_T2XCLK\_\_SHIFT EQU 000H ; Timer 2 External Clock Select

TMR2CN0\_T2XCLK\_\_SYSCLK\_DIV\_12 EQU 000H ; Timer 2 clock is the system clock divided by 12.

TMR2CN0\_T2XCLK\_\_EXTOSC\_DIV\_8 EQU 001H ; Timer 2 clock is the external oscillator divided

; by 8 (synchronized with SYSCLK when not in suspend

; or snooze mode).

TMR2CN0\_TR2\_\_BMASK EQU 004H ; Timer 2 Run Control

TMR2CN0\_TR2\_\_SHIFT EQU 002H ; Timer 2 Run Control

TMR2CN0\_TR2\_\_STOP EQU 000H ; Stop Timer 2.

TMR2CN0\_TR2\_\_RUN EQU 004H ; Start Timer 2 running.

TMR2CN0\_T2SPLIT\_\_BMASK EQU 008H ; Timer 2 Split Mode Enable

TMR2CN0\_T2SPLIT\_\_SHIFT EQU 003H ; Timer 2 Split Mode Enable

TMR2CN0\_T2SPLIT\_\_16\_BIT\_RELOAD EQU 000H ; Timer 2 operates in 16-bit auto-reload mode.

TMR2CN0\_T2SPLIT\_\_8\_BIT\_RELOAD EQU 008H ; Timer 2 operates as two 8-bit auto-reload timers.

TMR2CN0\_TF2CEN\_\_BMASK EQU 010H ; Timer 2 Capture Enable

TMR2CN0\_TF2CEN\_\_SHIFT EQU 004H ; Timer 2 Capture Enable

TMR2CN0\_TF2CEN\_\_DISABLED EQU 000H ; Disable capture mode.

TMR2CN0\_TF2CEN\_\_ENABLED EQU 010H ; Enable capture mode.

TMR2CN0\_TF2LEN\_\_BMASK EQU 020H ; Timer 2 Low Byte Interrupt Enable

TMR2CN0\_TF2LEN\_\_SHIFT EQU 005H ; Timer 2 Low Byte Interrupt Enable

TMR2CN0\_TF2LEN\_\_DISABLED EQU 000H ; Disable low byte interrupts.

TMR2CN0\_TF2LEN\_\_ENABLED EQU 020H ; Enable low byte interrupts.

TMR2CN0\_TF2L\_\_BMASK EQU 040H ; Timer 2 Low Byte Overflow Flag

TMR2CN0\_TF2L\_\_SHIFT EQU 006H ; Timer 2 Low Byte Overflow Flag

TMR2CN0\_TF2L\_\_NOT\_SET EQU 000H ; Timer 2 low byte did not overflow.

TMR2CN0\_TF2L\_\_SET EQU 040H ; Timer 2 low byte overflowed.

TMR2CN0\_TF2H\_\_BMASK EQU 080H ; Timer 2 High Byte Overflow Flag

TMR2CN0\_TF2H\_\_SHIFT EQU 007H ; Timer 2 High Byte Overflow Flag

TMR2CN0\_TF2H\_\_NOT\_SET EQU 000H ; Timer 2 8-bit high byte or 16-bit value did not

; overflow.

TMR2CN0\_TF2H\_\_SET EQU 080H ; Timer 2 8-bit high byte or 16-bit value

; overflowed.

;------------------------------------------------------------------------------

; TMR2CN1 Enums (Timer 2 Control 1 @ 0xFD)

;------------------------------------------------------------------------------

TMR2CN1\_T2CSEL\_\_FMASK EQU 007H ; Timer 2 Capture Select

TMR2CN1\_T2CSEL\_\_SHIFT EQU 000H ; Timer 2 Capture Select

TMR2CN1\_T2CSEL\_\_PIN EQU 000H ; Capture high-to-low transitions on the T2 input

; pin.

TMR2CN1\_T2CSEL\_\_LFOSC EQU 001H ; Capture high-to-low transitions of the LFO

; oscillator.

TMR2CN1\_T2CSEL\_\_COMPARATOR0 EQU 002H ; Capture high-to-low transitions of the Comparator

; 0 output.

TMR2CN1\_T2CSEL\_\_CLU0\_OUT EQU 004H ; Capture high-to-low transitions on the

; configurable logic unit 0 synchronous output.

TMR2CN1\_T2CSEL\_\_CLU1\_OUT EQU 005H ; Capture high-to-low transitions on the

; configurable logic unit 1 synchronous output.

TMR2CN1\_T2CSEL\_\_CLU2\_OUT EQU 006H ; Capture high-to-low transitions on the

; configurable logic unit 2 synchronous output.

TMR2CN1\_T2CSEL\_\_CLU3\_OUT EQU 007H ; Capture high-to-low transitions on the

; configurable logic unit 3 synchronous output.

TMR2CN1\_RLFSEL\_\_FMASK EQU 0E0H ; Force Reload Select

TMR2CN1\_RLFSEL\_\_SHIFT EQU 005H ; Force Reload Select

TMR2CN1\_RLFSEL\_\_NONE EQU 000H ; Timer will only reload on overflow events.

TMR2CN1\_RLFSEL\_\_CLU0\_OUT EQU 020H ; Timer will reload on overflow events and CLU0

; synchronous output high.

TMR2CN1\_RLFSEL\_\_CLU2\_OUT EQU 040H ; Timer will reload on overflow events and CLU2

; synchronous output high.

;------------------------------------------------------------------------------

; TMR2H Enums (Timer 2 High Byte @ 0xCF)

;------------------------------------------------------------------------------

TMR2H\_TMR2H\_\_FMASK EQU 0FFH ; Timer 2 High Byte

TMR2H\_TMR2H\_\_SHIFT EQU 000H ; Timer 2 High Byte

;------------------------------------------------------------------------------

; TMR2L Enums (Timer 2 Low Byte @ 0xCE)

;------------------------------------------------------------------------------

TMR2L\_TMR2L\_\_FMASK EQU 0FFH ; Timer 2 Low Byte

TMR2L\_TMR2L\_\_SHIFT EQU 000H ; Timer 2 Low Byte

;------------------------------------------------------------------------------

; TMR2RLH Enums (Timer 2 Reload High Byte @ 0xCB)

;------------------------------------------------------------------------------

TMR2RLH\_TMR2RLH\_\_FMASK EQU 0FFH ; Timer 2 Reload High Byte

TMR2RLH\_TMR2RLH\_\_SHIFT EQU 000H ; Timer 2 Reload High Byte

;------------------------------------------------------------------------------

; TMR2RLL Enums (Timer 2 Reload Low Byte @ 0xCA)

;------------------------------------------------------------------------------

TMR2RLL\_TMR2RLL\_\_FMASK EQU 0FFH ; Timer 2 Reload Low Byte

TMR2RLL\_TMR2RLL\_\_SHIFT EQU 000H ; Timer 2 Reload Low Byte

;------------------------------------------------------------------------------

; TMR3CN0 Enums (Timer 3 Control 0 @ 0x91)

;------------------------------------------------------------------------------

TMR3CN0\_T3XCLK\_\_FMASK EQU 003H ; Timer 3 External Clock Select

TMR3CN0\_T3XCLK\_\_SHIFT EQU 000H ; Timer 3 External Clock Select

TMR3CN0\_T3XCLK\_\_SYSCLK\_DIV\_12 EQU 000H ; Timer 3 clock is the system clock divided by 12.

TMR3CN0\_T3XCLK\_\_EXTOSC\_DIV\_8 EQU 001H ; Timer 3 clock is the external oscillator divided

; by 8 (synchronized with SYSCLK when not in suspend

; or snooze mode).

TMR3CN0\_T3XCLK\_\_LFOSC\_DIV\_8 EQU 003H ; Timer 3 clock is the low-frequency oscillator

; divided by 8 (synchronized with SYSCLK when not in

; suspend or snooze mode).

TMR3CN0\_TR3\_\_BMASK EQU 004H ; Timer 3 Run Control

TMR3CN0\_TR3\_\_SHIFT EQU 002H ; Timer 3 Run Control

TMR3CN0\_TR3\_\_STOP EQU 000H ; Stop Timer 3.

TMR3CN0\_TR3\_\_RUN EQU 004H ; Start Timer 3 running.

TMR3CN0\_T3SPLIT\_\_BMASK EQU 008H ; Timer 3 Split Mode Enable

TMR3CN0\_T3SPLIT\_\_SHIFT EQU 003H ; Timer 3 Split Mode Enable

TMR3CN0\_T3SPLIT\_\_16\_BIT\_RELOAD EQU 000H ; Timer 3 operates in 16-bit auto-reload mode.

TMR3CN0\_T3SPLIT\_\_8\_BIT\_RELOAD EQU 008H ; Timer 3 operates as two 8-bit auto-reload timers.

TMR3CN0\_TF3CEN\_\_BMASK EQU 010H ; Timer 3 Capture Enable

TMR3CN0\_TF3CEN\_\_SHIFT EQU 004H ; Timer 3 Capture Enable

TMR3CN0\_TF3CEN\_\_DISABLED EQU 000H ; Disable capture mode.

TMR3CN0\_TF3CEN\_\_ENABLED EQU 010H ; Enable capture mode.

TMR3CN0\_TF3LEN\_\_BMASK EQU 020H ; Timer 3 Low Byte Interrupt Enable

TMR3CN0\_TF3LEN\_\_SHIFT EQU 005H ; Timer 3 Low Byte Interrupt Enable

TMR3CN0\_TF3LEN\_\_DISABLED EQU 000H ; Disable low byte interrupts.

TMR3CN0\_TF3LEN\_\_ENABLED EQU 020H ; Enable low byte interrupts.

TMR3CN0\_TF3L\_\_BMASK EQU 040H ; Timer 3 Low Byte Overflow Flag

TMR3CN0\_TF3L\_\_SHIFT EQU 006H ; Timer 3 Low Byte Overflow Flag

TMR3CN0\_TF3L\_\_NOT\_SET EQU 000H ; Timer 3 low byte did not overflow.

TMR3CN0\_TF3L\_\_SET EQU 040H ; Timer 3 low byte overflowed.

TMR3CN0\_TF3H\_\_BMASK EQU 080H ; Timer 3 High Byte Overflow Flag

TMR3CN0\_TF3H\_\_SHIFT EQU 007H ; Timer 3 High Byte Overflow Flag

TMR3CN0\_TF3H\_\_NOT\_SET EQU 000H ; Timer 3 8-bit high byte or 16-bit value did not

; overflow.

TMR3CN0\_TF3H\_\_SET EQU 080H ; Timer 3 8-bit high byte or 16-bit value

; overflowed.

;------------------------------------------------------------------------------

; TMR3CN1 Enums (Timer 3 Control 1 @ 0xFE)

;------------------------------------------------------------------------------

TMR3CN1\_T3CSEL\_\_FMASK EQU 007H ; Timer 3 Capture Select

TMR3CN1\_T3CSEL\_\_SHIFT EQU 000H ; Timer 3 Capture Select

TMR3CN1\_T3CSEL\_\_PIN EQU 000H ; Capture high-to-low transitions on the T2 input

; pin.

TMR3CN1\_T3CSEL\_\_LFOSC EQU 001H ; Capture high-to-low transitions of the LFO

; oscillator.

TMR3CN1\_T3CSEL\_\_COMPARATOR0 EQU 002H ; Capture high-to-low transitions of the Comparator

; 0 output.

TMR3CN1\_T3CSEL\_\_CLU0\_OUT EQU 004H ; Capture high-to-low transitions on the

; configurable logic unit 0 synchronous output.

TMR3CN1\_T3CSEL\_\_CLU1\_OUT EQU 005H ; Capture high-to-low transitions on the

; configurable logic unit 1 synchronous output.

TMR3CN1\_T3CSEL\_\_CLU2\_OUT EQU 006H ; Capture high-to-low transitions on the

; configurable logic unit 2 synchronous output.

TMR3CN1\_T3CSEL\_\_CLU3\_OUT EQU 007H ; Capture high-to-low transitions on the

; configurable logic unit 3 synchronous output.

TMR3CN1\_STSYNC\_\_BMASK EQU 010H ; Suspend Timer Synchronization Status

TMR3CN1\_STSYNC\_\_SHIFT EQU 004H ; Suspend Timer Synchronization Status

TMR3CN1\_RLFSEL\_\_FMASK EQU 0E0H ; Force Reload Select

TMR3CN1\_RLFSEL\_\_SHIFT EQU 005H ; Force Reload Select

TMR3CN1\_RLFSEL\_\_SMB0\_SCL EQU 000H ; If the SMBTOE bit in the SMB0CF register is 0,

; then the timer will only reload on overflow

; events. If SMBTOE is 1, the timer will reload on

; overflow events and when the SMB0 SCL signal is

; high.

TMR3CN1\_RLFSEL\_\_CLU1\_OUT EQU 020H ; Timer will reload on overflow events and CLU1

; synchronous output high.

TMR3CN1\_RLFSEL\_\_CLU3\_OUT EQU 040H ; Timer will reload on overflow events and CLU3

; synchronous output high.

TMR3CN1\_RLFSEL\_\_NONE EQU 060H ; Timer will only reload on overflow events.

;------------------------------------------------------------------------------

; TMR3H Enums (Timer 3 High Byte @ 0x95)

;------------------------------------------------------------------------------

TMR3H\_TMR3H\_\_FMASK EQU 0FFH ; Timer 3 High Byte

TMR3H\_TMR3H\_\_SHIFT EQU 000H ; Timer 3 High Byte

;------------------------------------------------------------------------------

; TMR3L Enums (Timer 3 Low Byte @ 0x94)

;------------------------------------------------------------------------------

TMR3L\_TMR3L\_\_FMASK EQU 0FFH ; Timer 3 Low Byte

TMR3L\_TMR3L\_\_SHIFT EQU 000H ; Timer 3 Low Byte

;------------------------------------------------------------------------------

; TMR3RLH Enums (Timer 3 Reload High Byte @ 0x93)

;------------------------------------------------------------------------------

TMR3RLH\_TMR3RLH\_\_FMASK EQU 0FFH ; Timer 3 Reload High Byte

TMR3RLH\_TMR3RLH\_\_SHIFT EQU 000H ; Timer 3 Reload High Byte

;------------------------------------------------------------------------------

; TMR3RLL Enums (Timer 3 Reload Low Byte @ 0x92)

;------------------------------------------------------------------------------

TMR3RLL\_TMR3RLL\_\_FMASK EQU 0FFH ; Timer 3 Reload Low Byte

TMR3RLL\_TMR3RLL\_\_SHIFT EQU 000H ; Timer 3 Reload Low Byte

;------------------------------------------------------------------------------

; TMR4CN0 Enums (Timer 4 Control 0 @ 0x98)

;------------------------------------------------------------------------------

TMR4CN0\_T4XCLK\_\_FMASK EQU 003H ; Timer 4 External Clock Select

TMR4CN0\_T4XCLK\_\_SHIFT EQU 000H ; Timer 4 External Clock Select

TMR4CN0\_T4XCLK\_\_SYSCLK\_DIV\_12 EQU 000H ; Timer 4 clock is the system clock divided by 12.

TMR4CN0\_T4XCLK\_\_EXTOSC\_DIV\_8 EQU 001H ; Timer 4 clock is the external oscillator divided

; by 8 (synchronized with SYSCLK when not in suspend

; or snooze mode).

TMR4CN0\_T4XCLK\_\_TIMER3 EQU 002H ; Timer 4 is clocked by Timer 3 overflows.

TMR4CN0\_T4XCLK\_\_LFOSC\_DIV\_8 EQU 003H ; Timer 4 clock is the low-frequency oscillator

; divided by 8 (synchronized with SYSCLK when not in

; suspend or snooze mode).

TMR4CN0\_TR4\_\_BMASK EQU 004H ; Timer 4 Run Control

TMR4CN0\_TR4\_\_SHIFT EQU 002H ; Timer 4 Run Control

TMR4CN0\_TR4\_\_STOP EQU 000H ; Stop Timer 4.

TMR4CN0\_TR4\_\_RUN EQU 004H ; Start Timer 4 running.

TMR4CN0\_T4SPLIT\_\_BMASK EQU 008H ; Timer 4 Split Mode Enable

TMR4CN0\_T4SPLIT\_\_SHIFT EQU 003H ; Timer 4 Split Mode Enable

TMR4CN0\_T4SPLIT\_\_16\_BIT\_RELOAD EQU 000H ; Timer 4 operates in 16-bit auto-reload mode.

TMR4CN0\_T4SPLIT\_\_8\_BIT\_RELOAD EQU 008H ; Timer 4 operates as two 8-bit auto-reload timers.

TMR4CN0\_TF4CEN\_\_BMASK EQU 010H ; Timer 4 Capture Enable

TMR4CN0\_TF4CEN\_\_SHIFT EQU 004H ; Timer 4 Capture Enable

TMR4CN0\_TF4CEN\_\_DISABLED EQU 000H ; Disable capture mode.

TMR4CN0\_TF4CEN\_\_ENABLED EQU 010H ; Enable capture mode.

TMR4CN0\_TF4LEN\_\_BMASK EQU 020H ; Timer 4 Low Byte Interrupt Enable

TMR4CN0\_TF4LEN\_\_SHIFT EQU 005H ; Timer 4 Low Byte Interrupt Enable

TMR4CN0\_TF4LEN\_\_DISABLED EQU 000H ; Disable low byte interrupts.

TMR4CN0\_TF4LEN\_\_ENABLED EQU 020H ; Enable low byte interrupts.

TMR4CN0\_TF4L\_\_BMASK EQU 040H ; Timer 4 Low Byte Overflow Flag

TMR4CN0\_TF4L\_\_SHIFT EQU 006H ; Timer 4 Low Byte Overflow Flag

TMR4CN0\_TF4L\_\_NOT\_SET EQU 000H ; Timer 4 low byte did not overflow.

TMR4CN0\_TF4L\_\_SET EQU 040H ; Timer 4 low byte overflowed.

TMR4CN0\_TF4H\_\_BMASK EQU 080H ; Timer 4 High Byte Overflow Flag

TMR4CN0\_TF4H\_\_SHIFT EQU 007H ; Timer 4 High Byte Overflow Flag

TMR4CN0\_TF4H\_\_NOT\_SET EQU 000H ; Timer 4 8-bit high byte or 16-bit value did not

; overflow.

TMR4CN0\_TF4H\_\_SET EQU 080H ; Timer 4 8-bit high byte or 16-bit value

; overflowed.

;------------------------------------------------------------------------------

; TMR4CN1 Enums (Timer 4 Control 1 @ 0xFF)

;------------------------------------------------------------------------------

TMR4CN1\_T4CSEL\_\_FMASK EQU 007H ; Timer 4 Capture Select

TMR4CN1\_T4CSEL\_\_SHIFT EQU 000H ; Timer 4 Capture Select

TMR4CN1\_T4CSEL\_\_PIN EQU 000H ; Capture high-to-low transitions on the T2 input

; pin.

TMR4CN1\_T4CSEL\_\_LFOSC EQU 001H ; Capture high-to-low transitions of the LFO

; oscillator.

TMR4CN1\_T4CSEL\_\_COMPARATOR0 EQU 002H ; Capture high-to-low transitions of the Comparator

; 0 output.

TMR4CN1\_T4CSEL\_\_CLU0\_OUT EQU 004H ; Capture high-to-low transitions on the

; configurable logic unit 0 synchronous output.

TMR4CN1\_T4CSEL\_\_CLU1\_OUT EQU 005H ; Capture high-to-low transitions on the

; configurable logic unit 1 synchronous output.

TMR4CN1\_T4CSEL\_\_CLU2\_OUT EQU 006H ; Capture high-to-low transitions on the

; configurable logic unit 2 synchronous output.

TMR4CN1\_T4CSEL\_\_CLU3\_OUT EQU 007H ; Capture high-to-low transitions on the

; configurable logic unit 3 synchronous output.

TMR4CN1\_STSYNC\_\_BMASK EQU 010H ; Suspend Timer Synchronization Status

TMR4CN1\_STSYNC\_\_SHIFT EQU 004H ; Suspend Timer Synchronization Status

TMR4CN1\_RLFSEL\_\_FMASK EQU 0E0H ; Force Reload Select

TMR4CN1\_RLFSEL\_\_SHIFT EQU 005H ; Force Reload Select

TMR4CN1\_RLFSEL\_\_I2CSLAVE0\_SCL EQU 000H ; If the TIMEOUT bit in I2C0CN0 is 0, then the timer

; will only reload on overflow events. If TIMEOUT is

; 1, the timer will reload on overflow events and

; when the I2C0 SCL signal is high.

TMR4CN1\_RLFSEL\_\_CLU0\_OUT EQU 020H ; Timer will reload on overflow events and CLU0

; synchronous output high.

TMR4CN1\_RLFSEL\_\_CLU2\_OUT EQU 040H ; Timer will reload on overflow events and CLU2

; synchronous output high.

TMR4CN1\_RLFSEL\_\_NONE EQU 060H ; Timer will only reload on overflow events.

;------------------------------------------------------------------------------

; TMR4H Enums (Timer 4 High Byte @ 0xA5)

;------------------------------------------------------------------------------

TMR4H\_TMR4H\_\_FMASK EQU 0FFH ; Timer 4 High Byte

TMR4H\_TMR4H\_\_SHIFT EQU 000H ; Timer 4 High Byte

;------------------------------------------------------------------------------

; TMR4L Enums (Timer 4 Low Byte @ 0xA4)

;------------------------------------------------------------------------------

TMR4L\_TMR4L\_\_FMASK EQU 0FFH ; Timer 4 Low Byte

TMR4L\_TMR4L\_\_SHIFT EQU 000H ; Timer 4 Low Byte

;------------------------------------------------------------------------------

; TMR4RLH Enums (Timer 4 Reload High Byte @ 0xA3)

;------------------------------------------------------------------------------

TMR4RLH\_TMR4RLH\_\_FMASK EQU 0FFH ; Timer 4 Reload High Byte

TMR4RLH\_TMR4RLH\_\_SHIFT EQU 000H ; Timer 4 Reload High Byte

;------------------------------------------------------------------------------

; TMR4RLL Enums (Timer 4 Reload Low Byte @ 0xA2)

;------------------------------------------------------------------------------

TMR4RLL\_TMR4RLL\_\_FMASK EQU 0FFH ; Timer 4 Reload Low Byte

TMR4RLL\_TMR4RLL\_\_SHIFT EQU 000H ; Timer 4 Reload Low Byte

;------------------------------------------------------------------------------

; TMR5CN0 Enums (Timer 5 Control 0 @ 0xC0)

;------------------------------------------------------------------------------

TMR5CN0\_T5XCLK\_\_FMASK EQU 003H ; Timer 5 External Clock Select

TMR5CN0\_T5XCLK\_\_SHIFT EQU 000H ; Timer 5 External Clock Select

TMR5CN0\_T5XCLK\_\_SYSCLK\_DIV\_12 EQU 000H ; Timer 5 clock is the system clock divided by 12.

TMR5CN0\_T5XCLK\_\_EXTOSC\_DIV\_8 EQU 001H ; Timer 5 clock is the external oscillator divided

; by 8 (synchronized with SYSCLK when not in suspend

; or snooze mode).

TMR5CN0\_TR5\_\_BMASK EQU 004H ; Timer 5 Run Control

TMR5CN0\_TR5\_\_SHIFT EQU 002H ; Timer 5 Run Control

TMR5CN0\_TR5\_\_STOP EQU 000H ; Stop Timer 5.

TMR5CN0\_TR5\_\_RUN EQU 004H ; Start Timer 5 running.

TMR5CN0\_T5SPLIT\_\_BMASK EQU 008H ; Timer 5 Split Mode Enable

TMR5CN0\_T5SPLIT\_\_SHIFT EQU 003H ; Timer 5 Split Mode Enable

TMR5CN0\_T5SPLIT\_\_16\_BIT\_RELOAD EQU 000H ; Timer 5 operates in 16-bit auto-reload mode.

TMR5CN0\_T5SPLIT\_\_8\_BIT\_RELOAD EQU 008H ; Timer 5 operates as two 8-bit auto-reload timers.

TMR5CN0\_TF5CEN\_\_BMASK EQU 010H ; Timer 5 Capture Enable

TMR5CN0\_TF5CEN\_\_SHIFT EQU 004H ; Timer 5 Capture Enable

TMR5CN0\_TF5CEN\_\_DISABLED EQU 000H ; Disable capture mode.

TMR5CN0\_TF5CEN\_\_ENABLED EQU 010H ; Enable capture mode.

TMR5CN0\_TF5LEN\_\_BMASK EQU 020H ; Timer 5 Low Byte Interrupt Enable

TMR5CN0\_TF5LEN\_\_SHIFT EQU 005H ; Timer 5 Low Byte Interrupt Enable

TMR5CN0\_TF5LEN\_\_DISABLED EQU 000H ; Disable low byte interrupts.

TMR5CN0\_TF5LEN\_\_ENABLED EQU 020H ; Enable low byte interrupts.

TMR5CN0\_TF5L\_\_BMASK EQU 040H ; Timer 5 Low Byte Overflow Flag

TMR5CN0\_TF5L\_\_SHIFT EQU 006H ; Timer 5 Low Byte Overflow Flag

TMR5CN0\_TF5L\_\_NOT\_SET EQU 000H ; Timer 5 low byte did not overflow.

TMR5CN0\_TF5L\_\_SET EQU 040H ; Timer 5 low byte overflowed.

TMR5CN0\_TF5H\_\_BMASK EQU 080H ; Timer 5 High Byte Overflow Flag

TMR5CN0\_TF5H\_\_SHIFT EQU 007H ; Timer 5 High Byte Overflow Flag

TMR5CN0\_TF5H\_\_NOT\_SET EQU 000H ; Timer 5 8-bit high byte or 16-bit value did not

; overflow.

TMR5CN0\_TF5H\_\_SET EQU 080H ; Timer 5 8-bit high byte or 16-bit value

; overflowed.

;------------------------------------------------------------------------------

; TMR5CN1 Enums (Timer 5 Control 1 @ 0xF1)

;------------------------------------------------------------------------------

TMR5CN1\_T5CSEL\_\_FMASK EQU 007H ; Timer 5 Capture Select

TMR5CN1\_T5CSEL\_\_SHIFT EQU 000H ; Timer 5 Capture Select

TMR5CN1\_T5CSEL\_\_PIN EQU 000H ; Capture high-to-low transitions on the T2 input

; pin.

TMR5CN1\_T5CSEL\_\_LFOSC EQU 001H ; Capture high-to-low transitions of the LFO

; oscillator.

TMR5CN1\_T5CSEL\_\_COMPARATOR0 EQU 002H ; Capture high-to-low transitions of the Comparator

; 0 output.

TMR5CN1\_T5CSEL\_\_CLU0\_OUT EQU 004H ; Capture high-to-low transitions on the

; configurable logic unit 0 synchronous output.

TMR5CN1\_T5CSEL\_\_CLU1\_OUT EQU 005H ; Capture high-to-low transitions on the

; configurable logic unit 1 synchronous output.

TMR5CN1\_T5CSEL\_\_CLU2\_OUT EQU 006H ; Capture high-to-low transitions on the

; configurable logic unit 2 synchronous output.

TMR5CN1\_T5CSEL\_\_CLU3\_OUT EQU 007H ; Capture high-to-low transitions on the

; configurable logic unit 3 synchronous output.

TMR5CN1\_RLFSEL\_\_FMASK EQU 0E0H ; Force Reload Select

TMR5CN1\_RLFSEL\_\_SHIFT EQU 005H ; Force Reload Select

TMR5CN1\_RLFSEL\_\_NONE EQU 000H ; Timer will only reload on overflow events.

TMR5CN1\_RLFSEL\_\_CLU1\_OUT EQU 020H ; Timer will reload on overflow events and CLU1

; synchronous output high.

TMR5CN1\_RLFSEL\_\_CLU3\_OUT EQU 040H ; Timer will reload on overflow events and CLU3

; synchronous output high.

;------------------------------------------------------------------------------

; TMR5H Enums (Timer 5 High Byte @ 0xD5)

;------------------------------------------------------------------------------

TMR5H\_TMR5H\_\_FMASK EQU 0FFH ; Timer 5 High Byte

TMR5H\_TMR5H\_\_SHIFT EQU 000H ; Timer 5 High Byte

;------------------------------------------------------------------------------

; TMR5L Enums (Timer 5 Low Byte @ 0xD4)

;------------------------------------------------------------------------------

TMR5L\_TMR5L\_\_FMASK EQU 0FFH ; Timer 5 Low Byte

TMR5L\_TMR5L\_\_SHIFT EQU 000H ; Timer 5 Low Byte

;------------------------------------------------------------------------------

; TMR5RLH Enums (Timer 5 Reload High Byte @ 0xD3)

;------------------------------------------------------------------------------

TMR5RLH\_TMR5RLH\_\_FMASK EQU 0FFH ; Timer 5 Reload High Byte

TMR5RLH\_TMR5RLH\_\_SHIFT EQU 000H ; Timer 5 Reload High Byte

;------------------------------------------------------------------------------

; TMR5RLL Enums (Timer 5 Reload Low Byte @ 0xD2)

;------------------------------------------------------------------------------

TMR5RLL\_TMR5RLL\_\_FMASK EQU 0FFH ; Timer 5 Reload Low Byte

TMR5RLL\_TMR5RLL\_\_SHIFT EQU 000H ; Timer 5 Reload Low Byte

;------------------------------------------------------------------------------

; CKCON0 Enums (Clock Control 0 @ 0x8E)

;------------------------------------------------------------------------------

CKCON0\_SCA\_\_FMASK EQU 003H ; Timer 0/1 Prescale

CKCON0\_SCA\_\_SHIFT EQU 000H ; Timer 0/1 Prescale

CKCON0\_SCA\_\_SYSCLK\_DIV\_12 EQU 000H ; System clock divided by 12.

CKCON0\_SCA\_\_SYSCLK\_DIV\_4 EQU 001H ; System clock divided by 4.

CKCON0\_SCA\_\_SYSCLK\_DIV\_48 EQU 002H ; System clock divided by 48.

CKCON0\_SCA\_\_EXTOSC\_DIV\_8 EQU 003H ; External oscillator divided by 8 (synchronized

; with the system clock).

CKCON0\_T0M\_\_BMASK EQU 004H ; Timer 0 Clock Select

CKCON0\_T0M\_\_SHIFT EQU 002H ; Timer 0 Clock Select

CKCON0\_T0M\_\_PRESCALE EQU 000H ; Counter/Timer 0 uses the clock defined by the

; prescale field, SCA.

CKCON0\_T0M\_\_SYSCLK EQU 004H ; Counter/Timer 0 uses the system clock.

CKCON0\_T1M\_\_BMASK EQU 008H ; Timer 1 Clock Select

CKCON0\_T1M\_\_SHIFT EQU 003H ; Timer 1 Clock Select

CKCON0\_T1M\_\_PRESCALE EQU 000H ; Timer 1 uses the clock defined by the prescale

; field, SCA.

CKCON0\_T1M\_\_SYSCLK EQU 008H ; Timer 1 uses the system clock.

CKCON0\_T2ML\_\_BMASK EQU 010H ; Timer 2 Low Byte Clock Select

CKCON0\_T2ML\_\_SHIFT EQU 004H ; Timer 2 Low Byte Clock Select

CKCON0\_T2ML\_\_EXTERNAL\_CLOCK EQU 000H ; Timer 2 low byte uses the clock defined by T2XCLK

; in TMR2CN0.

CKCON0\_T2ML\_\_SYSCLK EQU 010H ; Timer 2 low byte uses the system clock.

CKCON0\_T2MH\_\_BMASK EQU 020H ; Timer 2 High Byte Clock Select

CKCON0\_T2MH\_\_SHIFT EQU 005H ; Timer 2 High Byte Clock Select

CKCON0\_T2MH\_\_EXTERNAL\_CLOCK EQU 000H ; Timer 2 high byte uses the clock defined by T2XCLK

; in TMR2CN0.

CKCON0\_T2MH\_\_SYSCLK EQU 020H ; Timer 2 high byte uses the system clock.

CKCON0\_T3ML\_\_BMASK EQU 040H ; Timer 3 Low Byte Clock Select

CKCON0\_T3ML\_\_SHIFT EQU 006H ; Timer 3 Low Byte Clock Select

CKCON0\_T3ML\_\_EXTERNAL\_CLOCK EQU 000H ; Timer 3 low byte uses the clock defined by T3XCLK

; in TMR3CN0.

CKCON0\_T3ML\_\_SYSCLK EQU 040H ; Timer 3 low byte uses the system clock.

CKCON0\_T3MH\_\_BMASK EQU 080H ; Timer 3 High Byte Clock Select

CKCON0\_T3MH\_\_SHIFT EQU 007H ; Timer 3 High Byte Clock Select

CKCON0\_T3MH\_\_EXTERNAL\_CLOCK EQU 000H ; Timer 3 high byte uses the clock defined by T3XCLK

; in TMR3CN0.

CKCON0\_T3MH\_\_SYSCLK EQU 080H ; Timer 3 high byte uses the system clock.

;------------------------------------------------------------------------------

; CKCON1 Enums (Clock Control 1 @ 0xA6)

;------------------------------------------------------------------------------

CKCON1\_T4ML\_\_BMASK EQU 001H ; Timer 4 Low Byte Clock Select

CKCON1\_T4ML\_\_SHIFT EQU 000H ; Timer 4 Low Byte Clock Select

CKCON1\_T4ML\_\_EXTERNAL\_CLOCK EQU 000H ; Timer 4 low byte uses the clock defined by T4XCLK

; in TMR4CN0.

CKCON1\_T4ML\_\_SYSCLK EQU 001H ; Timer 4 low byte uses the system clock.

CKCON1\_T4MH\_\_BMASK EQU 002H ; Timer 4 High Byte Clock Select

CKCON1\_T4MH\_\_SHIFT EQU 001H ; Timer 4 High Byte Clock Select

CKCON1\_T4MH\_\_EXTERNAL\_CLOCK EQU 000H ; Timer 4 high byte uses the clock defined by T4XCLK

; in TMR4CN0.

CKCON1\_T4MH\_\_SYSCLK EQU 002H ; Timer 4 high byte uses the system clock.

CKCON1\_T5ML\_\_BMASK EQU 004H ; Timer 5 Low Byte Clock Select

CKCON1\_T5ML\_\_SHIFT EQU 002H ; Timer 5 Low Byte Clock Select

CKCON1\_T5ML\_\_EXTERNAL\_CLOCK EQU 000H ; Timer 5 low byte uses the clock defined by T5XCLK

; in TMR5CN0.

CKCON1\_T5ML\_\_SYSCLK EQU 004H ; Timer 5 low byte uses the system clock.

CKCON1\_T5MH\_\_BMASK EQU 008H ; Timer 5 High Byte Clock Select

CKCON1\_T5MH\_\_SHIFT EQU 003H ; Timer 5 High Byte Clock Select

CKCON1\_T5MH\_\_EXTERNAL\_CLOCK EQU 000H ; Timer 5 high byte uses the clock defined by T5XCLK

; in TMR5CN0.

CKCON1\_T5MH\_\_SYSCLK EQU 008H ; Timer 5 high byte uses the system clock.

;------------------------------------------------------------------------------

; TCON Enums (Timer 0/1 Control @ 0x88)

;------------------------------------------------------------------------------

TCON\_IT0\_\_BMASK EQU 001H ; Interrupt 0 Type Select

TCON\_IT0\_\_SHIFT EQU 000H ; Interrupt 0 Type Select

TCON\_IT0\_\_LEVEL EQU 000H ; INT0 is level triggered.

TCON\_IT0\_\_EDGE EQU 001H ; INT0 is edge triggered.

TCON\_IE0\_\_BMASK EQU 002H ; External Interrupt 0

TCON\_IE0\_\_SHIFT EQU 001H ; External Interrupt 0

TCON\_IE0\_\_NOT\_SET EQU 000H ; Edge/level not detected.

TCON\_IE0\_\_SET EQU 002H ; Edge/level detected

TCON\_IT1\_\_BMASK EQU 004H ; Interrupt 1 Type Select

TCON\_IT1\_\_SHIFT EQU 002H ; Interrupt 1 Type Select

TCON\_IT1\_\_LEVEL EQU 000H ; INT1 is level triggered.

TCON\_IT1\_\_EDGE EQU 004H ; INT1 is edge triggered.

TCON\_IE1\_\_BMASK EQU 008H ; External Interrupt 1

TCON\_IE1\_\_SHIFT EQU 003H ; External Interrupt 1

TCON\_IE1\_\_NOT\_SET EQU 000H ; Edge/level not detected.

TCON\_IE1\_\_SET EQU 008H ; Edge/level detected

TCON\_TR0\_\_BMASK EQU 010H ; Timer 0 Run Control

TCON\_TR0\_\_SHIFT EQU 004H ; Timer 0 Run Control

TCON\_TR0\_\_STOP EQU 000H ; Stop Timer 0.

TCON\_TR0\_\_RUN EQU 010H ; Start Timer 0 running.

TCON\_TF0\_\_BMASK EQU 020H ; Timer 0 Overflow Flag

TCON\_TF0\_\_SHIFT EQU 005H ; Timer 0 Overflow Flag

TCON\_TF0\_\_NOT\_SET EQU 000H ; Timer 0 did not overflow.

TCON\_TF0\_\_SET EQU 020H ; Timer 0 overflowed.

TCON\_TR1\_\_BMASK EQU 040H ; Timer 1 Run Control

TCON\_TR1\_\_SHIFT EQU 006H ; Timer 1 Run Control

TCON\_TR1\_\_STOP EQU 000H ; Stop Timer 1.

TCON\_TR1\_\_RUN EQU 040H ; Start Timer 1 running.

TCON\_TF1\_\_BMASK EQU 080H ; Timer 1 Overflow Flag

TCON\_TF1\_\_SHIFT EQU 007H ; Timer 1 Overflow Flag

TCON\_TF1\_\_NOT\_SET EQU 000H ; Timer 1 did not overflow.

TCON\_TF1\_\_SET EQU 080H ; Timer 1 overflowed.

;------------------------------------------------------------------------------

; TMOD Enums (Timer 0/1 Mode @ 0x89)

;------------------------------------------------------------------------------

TMOD\_T0M\_\_FMASK EQU 003H ; Timer 0 Mode Select

TMOD\_T0M\_\_SHIFT EQU 000H ; Timer 0 Mode Select

TMOD\_T0M\_\_MODE0 EQU 000H ; Mode 0, 13-bit Counter/Timer

TMOD\_T0M\_\_MODE1 EQU 001H ; Mode 1, 16-bit Counter/Timer

TMOD\_T0M\_\_MODE2 EQU 002H ; Mode 2, 8-bit Counter/Timer with Auto-Reload

TMOD\_T0M\_\_MODE3 EQU 003H ; Mode 3, Two 8-bit Counter/Timers

TMOD\_CT0\_\_BMASK EQU 004H ; Counter/Timer 0 Select

TMOD\_CT0\_\_SHIFT EQU 002H ; Counter/Timer 0 Select

TMOD\_CT0\_\_TIMER EQU 000H ; Timer Mode. Timer 0 increments on the clock

; defined by T0M in the CKCON0 register.

TMOD\_CT0\_\_COUNTER EQU 004H ; Counter Mode. Timer 0 increments on high-to-low

; transitions of an external pin (T0).

TMOD\_GATE0\_\_BMASK EQU 008H ; Timer 0 Gate Control

TMOD\_GATE0\_\_SHIFT EQU 003H ; Timer 0 Gate Control

TMOD\_GATE0\_\_DISABLED EQU 000H ; Timer 0 enabled when TR0 = 1 irrespective of INT0

; logic level.

TMOD\_GATE0\_\_ENABLED EQU 008H ; Timer 0 enabled only when TR0 = 1 and INT0 is

; active as defined by bit IN0PL in register IT01CF.

TMOD\_T1M\_\_FMASK EQU 030H ; Timer 1 Mode Select

TMOD\_T1M\_\_SHIFT EQU 004H ; Timer 1 Mode Select

TMOD\_T1M\_\_MODE0 EQU 000H ; Mode 0, 13-bit Counter/Timer

TMOD\_T1M\_\_MODE1 EQU 010H ; Mode 1, 16-bit Counter/Timer

TMOD\_T1M\_\_MODE2 EQU 020H ; Mode 2, 8-bit Counter/Timer with Auto-Reload

TMOD\_T1M\_\_MODE3 EQU 030H ; Mode 3, Timer 1 Inactive

TMOD\_CT1\_\_BMASK EQU 040H ; Counter/Timer 1 Select

TMOD\_CT1\_\_SHIFT EQU 006H ; Counter/Timer 1 Select

TMOD\_CT1\_\_TIMER EQU 000H ; Timer Mode. Timer 1 increments on the clock

; defined by T1M in the CKCON0 register.

TMOD\_CT1\_\_COUNTER EQU 040H ; Counter Mode. Timer 1 increments on high-to-low

; transitions of an external pin (T1).

TMOD\_GATE1\_\_BMASK EQU 080H ; Timer 1 Gate Control

TMOD\_GATE1\_\_SHIFT EQU 007H ; Timer 1 Gate Control

TMOD\_GATE1\_\_DISABLED EQU 000H ; Timer 1 enabled when TR1 = 1 irrespective of INT1

; logic level.

TMOD\_GATE1\_\_ENABLED EQU 080H ; Timer 1 enabled only when TR1 = 1 and INT1 is

; active as defined by bit IN1PL in register IT01CF.

;------------------------------------------------------------------------------

; SBCON1 Enums (UART1 Baud Rate Generator Control @ 0x94)

;------------------------------------------------------------------------------

SBCON1\_BPS\_\_FMASK EQU 007H ; Baud Rate Prescaler Select

SBCON1\_BPS\_\_SHIFT EQU 000H ; Baud Rate Prescaler Select

SBCON1\_BPS\_\_DIV\_BY\_12 EQU 000H ; Prescaler = 12.

SBCON1\_BPS\_\_DIV\_BY\_4 EQU 001H ; Prescaler = 4.

SBCON1\_BPS\_\_DIV\_BY\_48 EQU 002H ; Prescaler = 48.

SBCON1\_BPS\_\_DIV\_BY\_1 EQU 003H ; Prescaler = 1.

SBCON1\_BPS\_\_DIV\_BY\_8 EQU 004H ; Prescaler = 8.

SBCON1\_BPS\_\_DIV\_BY\_16 EQU 005H ; Prescaler = 16.

SBCON1\_BPS\_\_DIV\_BY\_24 EQU 006H ; Prescaler = 24.

SBCON1\_BPS\_\_DIV\_BY\_32 EQU 007H ; Prescaler = 32.

SBCON1\_BREN\_\_BMASK EQU 040H ; Baud Rate Generator Enable

SBCON1\_BREN\_\_SHIFT EQU 006H ; Baud Rate Generator Enable

SBCON1\_BREN\_\_DISABLED EQU 000H ; Disable the baud rate generator. UART1 will not

; function.

SBCON1\_BREN\_\_ENABLED EQU 040H ; Enable the baud rate generator.

;------------------------------------------------------------------------------

; SBRLH1 Enums (UART1 Baud Rate Generator High Byte @ 0x96)

;------------------------------------------------------------------------------

SBRLH1\_BRH\_\_FMASK EQU 0FFH ; UART1 Baud Rate Reload High

SBRLH1\_BRH\_\_SHIFT EQU 000H ; UART1 Baud Rate Reload High

;------------------------------------------------------------------------------

; SBRLL1 Enums (UART1 Baud Rate Generator Low Byte @ 0x95)

;------------------------------------------------------------------------------

SBRLL1\_BRL\_\_FMASK EQU 0FFH ; UART1 Baud Rate Reload Low

SBRLL1\_BRL\_\_SHIFT EQU 000H ; UART1 Baud Rate Reload Low

;------------------------------------------------------------------------------

; SBUF1 Enums (UART1 Serial Port Data Buffer @ 0x92)

;------------------------------------------------------------------------------

SBUF1\_SBUF1\_\_FMASK EQU 0FFH ; Serial Port Data Buffer

SBUF1\_SBUF1\_\_SHIFT EQU 000H ; Serial Port Data Buffer

;------------------------------------------------------------------------------

; SCON1 Enums (UART1 Serial Port Control @ 0xC8)

;------------------------------------------------------------------------------

SCON1\_RI\_\_BMASK EQU 001H ; Receive Interrupt Flag

SCON1\_RI\_\_SHIFT EQU 000H ; Receive Interrupt Flag

SCON1\_RI\_\_NOT\_SET EQU 000H ; New data has not been received by UART1.

SCON1\_RI\_\_SET EQU 001H ; UART1 received one or more data bytes.

SCON1\_TI\_\_BMASK EQU 002H ; Transmit Interrupt Flag

SCON1\_TI\_\_SHIFT EQU 001H ; Transmit Interrupt Flag

SCON1\_TI\_\_NOT\_SET EQU 000H ; A byte of data has not been transmitted by UART1.

SCON1\_TI\_\_SET EQU 002H ; UART1 transmitted a byte of data.

SCON1\_RBX\_\_BMASK EQU 004H ; Extra Receive Bit

SCON1\_RBX\_\_SHIFT EQU 002H ; Extra Receive Bit

SCON1\_RBX\_\_LOW EQU 000H ; The extra bit or the first stop bit is 0.

SCON1\_RBX\_\_HIGH EQU 004H ; The extra bit or the first stop bit is 1.

SCON1\_TBX\_\_BMASK EQU 008H ; Extra Transmission Bit

SCON1\_TBX\_\_SHIFT EQU 003H ; Extra Transmission Bit

SCON1\_TBX\_\_LOW EQU 000H ; Set extra bit to 0 (low).

SCON1\_TBX\_\_HIGH EQU 008H ; Set extra bit to 1 (high).

SCON1\_REN\_\_BMASK EQU 010H ; Receive Enable

SCON1\_REN\_\_SHIFT EQU 004H ; Receive Enable

SCON1\_REN\_\_RECEIVE\_DISABLED EQU 000H ; UART1 reception disabled.

SCON1\_REN\_\_RECEIVE\_ENABLED EQU 010H ; UART1 reception enabled.

SCON1\_PERR\_\_BMASK EQU 040H ; Parity Error Flag

SCON1\_PERR\_\_SHIFT EQU 006H ; Parity Error Flag

SCON1\_PERR\_\_NOT\_SET EQU 000H ; Parity error has not occurred.

SCON1\_PERR\_\_SET EQU 040H ; Parity error has occurred.

SCON1\_OVR\_\_BMASK EQU 080H ; Receive FIFO Overrun Flag

SCON1\_OVR\_\_SHIFT EQU 007H ; Receive FIFO Overrun Flag

SCON1\_OVR\_\_NOT\_SET EQU 000H ; Receive FIFO overrun has not occurred.

SCON1\_OVR\_\_SET EQU 080H ; Receive FIFO overrun has occurred.

;------------------------------------------------------------------------------

; SMOD1 Enums (UART1 Mode @ 0x93)

;------------------------------------------------------------------------------

SMOD1\_SBL\_\_BMASK EQU 001H ; Stop Bit Length

SMOD1\_SBL\_\_SHIFT EQU 000H ; Stop Bit Length

SMOD1\_SBL\_\_SHORT EQU 000H ; Short: Stop bit is active for one bit time.

SMOD1\_SBL\_\_LONG EQU 001H ; Long: Stop bit is active for two bit times (data

; length = 6, 7, or 8 bits) or 1.5 bit times (data

; length = 5 bits).

SMOD1\_XBE\_\_BMASK EQU 002H ; Extra Bit Enable

SMOD1\_XBE\_\_SHIFT EQU 001H ; Extra Bit Enable

SMOD1\_XBE\_\_DISABLED EQU 000H ; Disable the extra bit.

SMOD1\_XBE\_\_ENABLED EQU 002H ; Enable the extra bit.

SMOD1\_SDL\_\_FMASK EQU 00CH ; Data Length

SMOD1\_SDL\_\_SHIFT EQU 002H ; Data Length

SMOD1\_SDL\_\_5\_BITS EQU 000H ; 5 bits.

SMOD1\_SDL\_\_6\_BITS EQU 004H ; 6 bits.

SMOD1\_SDL\_\_7\_BITS EQU 008H ; 7 bits.

SMOD1\_SDL\_\_8\_BITS EQU 00CH ; 8 bits.

SMOD1\_PE\_\_BMASK EQU 010H ; Parity Enable

SMOD1\_PE\_\_SHIFT EQU 004H ; Parity Enable

SMOD1\_PE\_\_PARITY\_DISABLED EQU 000H ; Disable hardware parity.

SMOD1\_PE\_\_PARITY\_ENABLED EQU 010H ; Enable hardware parity.

SMOD1\_SPT\_\_FMASK EQU 060H ; Parity Type

SMOD1\_SPT\_\_SHIFT EQU 005H ; Parity Type

SMOD1\_SPT\_\_ODD\_PARITY EQU 000H ; Odd.

SMOD1\_SPT\_\_EVEN\_PARITY EQU 020H ; Even.

SMOD1\_SPT\_\_MARK\_PARITY EQU 040H ; Mark.

SMOD1\_SPT\_\_SPACE\_PARITY EQU 060H ; Space.

SMOD1\_MCE\_\_BMASK EQU 080H ; Multiprocessor Communication Enable

SMOD1\_MCE\_\_SHIFT EQU 007H ; Multiprocessor Communication Enable

SMOD1\_MCE\_\_MULTI\_DISABLED EQU 000H ; RI will be activated if the stop bits are 1.

SMOD1\_MCE\_\_MULTI\_ENABLED EQU 080H ; RI will be activated if the stop bits and extra

; bit are 1. The extra bit must be enabled using

; XBE.

;------------------------------------------------------------------------------

; UART1FCN0 Enums (UART1 FIFO Control 0 @ 0x9D)

;------------------------------------------------------------------------------

UART1FCN0\_RXTH\_\_FMASK EQU 003H ; RX FIFO Threshold

UART1FCN0\_RXTH\_\_SHIFT EQU 000H ; RX FIFO Threshold

UART1FCN0\_RXTH\_\_ZERO EQU 000H ; RFRQ will be set anytime new data arrives in the

; RX FIFO (when the RX FIFO is not empty).

UART1FCN0\_RFLSH\_\_BMASK EQU 004H ; RX FIFO Flush

UART1FCN0\_RFLSH\_\_SHIFT EQU 002H ; RX FIFO Flush

UART1FCN0\_RFLSH\_\_FLUSH EQU 004H ; Initiate an RX FIFO flush.

UART1FCN0\_RFRQE\_\_BMASK EQU 008H ; Read Request Interrupt Enable

UART1FCN0\_RFRQE\_\_SHIFT EQU 003H ; Read Request Interrupt Enable

UART1FCN0\_RFRQE\_\_DISABLED EQU 000H ; UART1 interrupts will not be generated when RFRQ

; is set.

UART1FCN0\_RFRQE\_\_ENABLED EQU 008H ; UART1 interrupts will be generated if RFRQ is set.

UART1FCN0\_TXTH\_\_FMASK EQU 030H ; TX FIFO Threshold

UART1FCN0\_TXTH\_\_SHIFT EQU 004H ; TX FIFO Threshold

UART1FCN0\_TXTH\_\_ZERO EQU 000H ; TFRQ will be set when the TX FIFO is empty.

UART1FCN0\_TFLSH\_\_BMASK EQU 040H ; TX FIFO Flush

UART1FCN0\_TFLSH\_\_SHIFT EQU 006H ; TX FIFO Flush

UART1FCN0\_TFLSH\_\_FLUSH EQU 040H ; Initiate a TX FIFO flush.

UART1FCN0\_TFRQE\_\_BMASK EQU 080H ; Write Request Interrupt Enable

UART1FCN0\_TFRQE\_\_SHIFT EQU 007H ; Write Request Interrupt Enable

UART1FCN0\_TFRQE\_\_DISABLED EQU 000H ; UART1 interrupts will not be generated when TFRQ

; is set.

UART1FCN0\_TFRQE\_\_ENABLED EQU 080H ; UART1 interrupts will be generated if TFRQ is set.

;------------------------------------------------------------------------------

; UART1FCN1 Enums (UART1 FIFO Control 1 @ 0xD8)

;------------------------------------------------------------------------------

UART1FCN1\_RIE\_\_BMASK EQU 001H ; Receive Interrupt Enable

UART1FCN1\_RIE\_\_SHIFT EQU 000H ; Receive Interrupt Enable

UART1FCN1\_RIE\_\_DISABLED EQU 000H ; The RI flag will not generate UART1 interrupts.

UART1FCN1\_RIE\_\_ENABLED EQU 001H ; The RI flag will generate UART1 interrupts when it

; is set.

UART1FCN1\_RXTO\_\_FMASK EQU 006H ; Receive Timeout

UART1FCN1\_RXTO\_\_SHIFT EQU 001H ; Receive Timeout

UART1FCN1\_RXTO\_\_DISABLED EQU 000H ; The receive timeout feature is disabled.

UART1FCN1\_RXTO\_\_TIMEOUT\_2 EQU 002H ; A receive timeout will occur after 2 idle periods

; on the UART RX line.

UART1FCN1\_RXTO\_\_TIMEOUT\_4 EQU 004H ; A receive timeout will occur after 4 idle periods

; on the UART RX line.

UART1FCN1\_RXTO\_\_TIMEOUT\_16 EQU 006H ; A receive timeout will occur after 16 idle periods

; on the UART RX line.

UART1FCN1\_RFRQ\_\_BMASK EQU 008H ; Receive FIFO Request

UART1FCN1\_RFRQ\_\_SHIFT EQU 003H ; Receive FIFO Request

UART1FCN1\_RFRQ\_\_NOT\_SET EQU 000H ; The number of bytes in the RX FIFO is less than or

; equal to RXTH.

UART1FCN1\_RFRQ\_\_SET EQU 008H ; The number of bytes in the RX FIFO is greater than

; RXTH.

UART1FCN1\_TIE\_\_BMASK EQU 010H ; Transmit Interrupt Enable

UART1FCN1\_TIE\_\_SHIFT EQU 004H ; Transmit Interrupt Enable

UART1FCN1\_TIE\_\_DISABLED EQU 000H ; The TI flag will not generate UART1 interrupts.

UART1FCN1\_TIE\_\_ENABLED EQU 010H ; The TI flag will generate UART1 interrupts when it

; is set.

UART1FCN1\_TXHOLD\_\_BMASK EQU 020H ; Transmit Hold

UART1FCN1\_TXHOLD\_\_SHIFT EQU 005H ; Transmit Hold

UART1FCN1\_TXHOLD\_\_CONTINUE EQU 000H ; The UART will continue to transmit any available

; data in the TX FIFO.

UART1FCN1\_TXHOLD\_\_HOLD EQU 020H ; The UART will not transmit any new data from the

; TX FIFO.

UART1FCN1\_TXNF\_\_BMASK EQU 040H ; TX FIFO Not Full

UART1FCN1\_TXNF\_\_SHIFT EQU 006H ; TX FIFO Not Full

UART1FCN1\_TXNF\_\_FULL EQU 000H ; The TX FIFO is full.

UART1FCN1\_TXNF\_\_NOT\_FULL EQU 040H ; The TX FIFO has room for more data.

UART1FCN1\_TFRQ\_\_BMASK EQU 080H ; Transmit FIFO Request

UART1FCN1\_TFRQ\_\_SHIFT EQU 007H ; Transmit FIFO Request

UART1FCN1\_TFRQ\_\_NOT\_SET EQU 000H ; The number of bytes in the TX FIFO is greater than

; TXTH.

UART1FCN1\_TFRQ\_\_SET EQU 080H ; The number of bytes in the TX FIFO is less than or

; equal to TXTH.

;------------------------------------------------------------------------------

; UART1FCT Enums (UART1 FIFO Count @ 0xFA)

;------------------------------------------------------------------------------

UART1FCT\_RXCNT\_\_FMASK EQU 007H ; RX FIFO Count

UART1FCT\_RXCNT\_\_SHIFT EQU 000H ; RX FIFO Count

UART1FCT\_TXCNT\_\_FMASK EQU 070H ; TX FIFO Count

UART1FCT\_TXCNT\_\_SHIFT EQU 004H ; TX FIFO Count

;------------------------------------------------------------------------------

; UART1LIN Enums (UART1 LIN Configuration @ 0x9E)

;------------------------------------------------------------------------------

UART1LIN\_SYNCDIE\_\_BMASK EQU 001H ; LIN Sync Detect Interrupt Enable

UART1LIN\_SYNCDIE\_\_SHIFT EQU 000H ; LIN Sync Detect Interrupt Enable

UART1LIN\_SYNCDIE\_\_DISABLED EQU 000H ; The SYNCD flag will not generate UART1 interrupts.

UART1LIN\_SYNCDIE\_\_ENABLED EQU 001H ; The SYNCD flag will generate UART1 interrupts when

; it is set.

UART1LIN\_SYNCTOIE\_\_BMASK EQU 002H ; LIN Sync Detect Timeout Interrupt Enable

UART1LIN\_SYNCTOIE\_\_SHIFT EQU 001H ; LIN Sync Detect Timeout Interrupt Enable

UART1LIN\_SYNCTOIE\_\_DISABLED EQU 000H ; The SYNCTO flag will not generate UART1

; interrupts.

UART1LIN\_SYNCTOIE\_\_ENABLED EQU 002H ; The SYNCTO flag will generate UART1 interrupts

; when it is set.

UART1LIN\_BREAKDNIE\_\_BMASK EQU 004H ; LIN Break Done Interrupt Enable

UART1LIN\_BREAKDNIE\_\_SHIFT EQU 002H ; LIN Break Done Interrupt Enable

UART1LIN\_BREAKDNIE\_\_DISABLED EQU 000H ; The BREAKDN flag will not generate UART1

; interrupts.

UART1LIN\_BREAKDNIE\_\_ENABLED EQU 004H ; The BREAKDN flag will generate UART1 interrupts

; when it is set.

UART1LIN\_LINMDE\_\_BMASK EQU 008H ; LIN Mode Enable

UART1LIN\_LINMDE\_\_SHIFT EQU 003H ; LIN Mode Enable

UART1LIN\_LINMDE\_\_DISABLED EQU 000H ; If AUTOBDE is set to 1, sync detection and

; autobaud will begin on the first falling edge of

; RX.

UART1LIN\_LINMDE\_\_ENABLED EQU 008H ; A valid LIN break field and delimiter must be

; detected prior to the hardware state machine

; recognizing a sync word and performing autobaud.

UART1LIN\_SYNCD\_\_BMASK EQU 010H ; LIN Sync Detect Flag

UART1LIN\_SYNCD\_\_SHIFT EQU 004H ; LIN Sync Detect Flag

UART1LIN\_SYNCD\_\_NOT\_SET EQU 000H ; A sync has not been detected or is not yet

; complete.

UART1LIN\_SYNCD\_\_SYNC\_DONE EQU 010H ; A valid sync word was detected.

UART1LIN\_SYNCTO\_\_BMASK EQU 020H ; LIN Sync Timeout Flag

UART1LIN\_SYNCTO\_\_SHIFT EQU 005H ; LIN Sync Timeout Flag

UART1LIN\_SYNCTO\_\_NOT\_SET EQU 000H ; A sync timeout has not occured.

UART1LIN\_SYNCTO\_\_TIMEOUT EQU 020H ; A sync timeout occured.

UART1LIN\_BREAKDN\_\_BMASK EQU 040H ; LIN Break Done Flag

UART1LIN\_BREAKDN\_\_SHIFT EQU 006H ; LIN Break Done Flag

UART1LIN\_BREAKDN\_\_NOT\_SET EQU 000H ; A LIN break has not been detected.

UART1LIN\_BREAKDN\_\_BREAK EQU 040H ; A LIN break was detected since the flag was last

; cleared.

UART1LIN\_AUTOBDE\_\_BMASK EQU 080H ; Auto Baud Detection Enable

UART1LIN\_AUTOBDE\_\_SHIFT EQU 007H ; Auto Baud Detection Enable

UART1LIN\_AUTOBDE\_\_DISABLED EQU 000H ; Autobaud is not enabled.

UART1LIN\_AUTOBDE\_\_ENABLED EQU 080H ; Autobaud is enabled.

;------------------------------------------------------------------------------

; UART1PCF Enums (UART1 Pin Configuration @ 0xDA)

;------------------------------------------------------------------------------

UART1PCF\_RXSEL\_\_FMASK EQU 003H ; RX Input Select

UART1PCF\_RXSEL\_\_SHIFT EQU 000H ; RX Input Select

UART1PCF\_RXSEL\_\_CROSSBAR EQU 000H ; RX is connected to the pin assigned by the

; crossbar.

UART1PCF\_RXSEL\_\_CLU0 EQU 001H ; RX is connected to the CLU0 output signal.

UART1PCF\_RXSEL\_\_CLU1 EQU 002H ; RX is connected to the CLU1 output signal.

UART1PCF\_RXSEL\_\_CLU2 EQU 003H ; RX is connected to the CLU2 output signal.

;------------------------------------------------------------------------------

; SBUF0 Enums (UART0 Serial Port Data Buffer @ 0x99)

;------------------------------------------------------------------------------

SBUF0\_SBUF0\_\_FMASK EQU 0FFH ; Serial Data Buffer

SBUF0\_SBUF0\_\_SHIFT EQU 000H ; Serial Data Buffer

;------------------------------------------------------------------------------

; SCON0 Enums (UART0 Serial Port Control @ 0x98)

;------------------------------------------------------------------------------

SCON0\_RI\_\_BMASK EQU 001H ; Receive Interrupt Flag

SCON0\_RI\_\_SHIFT EQU 000H ; Receive Interrupt Flag

SCON0\_RI\_\_NOT\_SET EQU 000H ; New data has not been received by UART0.

SCON0\_RI\_\_SET EQU 001H ; UART0 received one or more data bytes.

SCON0\_TI\_\_BMASK EQU 002H ; Transmit Interrupt Flag

SCON0\_TI\_\_SHIFT EQU 001H ; Transmit Interrupt Flag

SCON0\_TI\_\_NOT\_SET EQU 000H ; A byte of data has not been transmitted by UART0.

SCON0\_TI\_\_SET EQU 002H ; UART0 transmitted a byte of data.

SCON0\_RB8\_\_BMASK EQU 004H ; Ninth Receive Bit

SCON0\_RB8\_\_SHIFT EQU 002H ; Ninth Receive Bit

SCON0\_RB8\_\_NOT\_SET EQU 000H ; In Mode 0, the STOP bit was 0. In Mode 1, the 9th

; bit was 0.

SCON0\_RB8\_\_SET EQU 004H ; In Mode 0, the STOP bit was 1. In Mode 1, the 9th

; bit was 1.

SCON0\_TB8\_\_BMASK EQU 008H ; Ninth Transmission Bit

SCON0\_TB8\_\_SHIFT EQU 003H ; Ninth Transmission Bit

SCON0\_TB8\_\_NOT\_SET EQU 000H ; In Mode 1, set the 9th transmission bit to 0.

SCON0\_TB8\_\_SET EQU 008H ; In Mode 1, set the 9th transmission bit to 1.

SCON0\_REN\_\_BMASK EQU 010H ; Receive Enable

SCON0\_REN\_\_SHIFT EQU 004H ; Receive Enable

SCON0\_REN\_\_RECEIVE\_DISABLED EQU 000H ; UART0 reception disabled.

SCON0\_REN\_\_RECEIVE\_ENABLED EQU 010H ; UART0 reception enabled.

SCON0\_MCE\_\_BMASK EQU 020H ; Multiprocessor Communication Enable

SCON0\_MCE\_\_SHIFT EQU 005H ; Multiprocessor Communication Enable

SCON0\_MCE\_\_MULTI\_DISABLED EQU 000H ; Ignore level of 9th bit / Stop bit.

SCON0\_MCE\_\_MULTI\_ENABLED EQU 020H ; RI is set and an interrupt is generated only when

; the stop bit is logic 1 (Mode 0) or when the 9th

; bit is logic 1 (Mode 1).

SCON0\_SMODE\_\_BMASK EQU 080H ; Serial Port 0 Operation Mode

SCON0\_SMODE\_\_SHIFT EQU 007H ; Serial Port 0 Operation Mode

SCON0\_SMODE\_\_8\_BIT EQU 000H ; 8-bit UART with Variable Baud Rate (Mode 0).

SCON0\_SMODE\_\_9\_BIT EQU 080H ; 9-bit UART with Variable Baud Rate (Mode 1).

;------------------------------------------------------------------------------

; UART0PCF Enums (UART0 Pin Configuration @ 0xD9)

;------------------------------------------------------------------------------

UART0PCF\_RXSEL\_\_FMASK EQU 003H ; RX Input Select

UART0PCF\_RXSEL\_\_SHIFT EQU 000H ; RX Input Select

UART0PCF\_RXSEL\_\_CROSSBAR EQU 000H ; RX is connected to the pin assigned by the

; crossbar.

UART0PCF\_RXSEL\_\_CLU0 EQU 001H ; RX is connected to the CLU0 output signal.

UART0PCF\_RXSEL\_\_CLU1 EQU 002H ; RX is connected to the CLU1 output signal.

UART0PCF\_RXSEL\_\_CLU2 EQU 003H ; RX is connected to the CLU2 output signal.

;------------------------------------------------------------------------------

; VDM0CN Enums (Supply Monitor Control @ 0xFF)

;------------------------------------------------------------------------------

VDM0CN\_VDDSTAT\_\_BMASK EQU 040H ; Supply Status

VDM0CN\_VDDSTAT\_\_SHIFT EQU 006H ; Supply Status

VDM0CN\_VDDSTAT\_\_BELOW EQU 000H ; VDD is at or below the supply monitor threshold.

VDM0CN\_VDDSTAT\_\_ABOVE EQU 040H ; VDD is above the supply monitor threshold.

VDM0CN\_VDMEN\_\_BMASK EQU 080H ; Supply Monitor Enable

VDM0CN\_VDMEN\_\_SHIFT EQU 007H ; Supply Monitor Enable

VDM0CN\_VDMEN\_\_DISABLED EQU 000H ; Supply Monitor Disabled.

VDM0CN\_VDMEN\_\_ENABLED EQU 080H ; Supply Monitor Enabled.

;------------------------------------------------------------------------------

; REF0CN Enums (Voltage Reference Control @ 0xD1)

;------------------------------------------------------------------------------

REF0CN\_VREFSL\_\_FMASK EQU 0C0H ; Voltage Reference Output Select

REF0CN\_VREFSL\_\_SHIFT EQU 006H ; Voltage Reference Output Select

REF0CN\_VREFSL\_\_NONE EQU 000H ; The VREF pin is not driven by an on-chip

; reference. It may be driven with an external

; reference.

REF0CN\_VREFSL\_\_VREF\_1P2 EQU 040H ; 1.2 V reference output to VREF pin.

REF0CN\_VREFSL\_\_VREF\_2P4 EQU 080H ; 2.4 V reference output to VREF pin.

;------------------------------------------------------------------------------

; REG0CN Enums (Voltage Regulator 0 Control @ 0xC9)

;------------------------------------------------------------------------------

REG0CN\_STOPCF\_\_BMASK EQU 008H ; Stop and Shutdown Mode Configuration

REG0CN\_STOPCF\_\_SHIFT EQU 003H ; Stop and Shutdown Mode Configuration

REG0CN\_STOPCF\_\_ACTIVE EQU 000H ; Regulator is still active in stop mode. Any

; enabled reset source will reset the device.

REG0CN\_STOPCF\_\_SHUTDOWN EQU 008H ; Regulator is shut down in stop mode (device enters

; Shutdown mode). Only the RSTb pin or power cycle

; can reset the device.

;------------------------------------------------------------------------------

; WDTCN Enums (Watchdog Timer Control @ 0x97)

;------------------------------------------------------------------------------

WDTCN\_WDTCN\_\_FMASK EQU 0FFH ; WDT Control

WDTCN\_WDTCN\_\_SHIFT EQU 000H ; WDT Control

;------------------------------------------------------------------------------

; EMI0CN Enums (External Memory Interface Control @ 0xE7)

;------------------------------------------------------------------------------

EMI0CN\_PGSEL\_\_FMASK EQU 00FH ; XRAM Page Select

EMI0CN\_PGSEL\_\_SHIFT EQU 000H ; XRAM Page Select